

MS7004V300

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CPU:

Intel Northwood/Prescott
Up to 3.6GHz

System Chipset:

P4X533/PT800 (North Bridge)
VIA 8237 (South Bridge)

On Board Chipset:

BIOS -- ISA EEPROM
AC'97 Codec --ALC655
LPC Super I/O -- W83697HF
LAN -- PCI RTL8100C
CLOCK -- CY28341-3

Main Memory:

DDR * 2 (Max 2GB)

Expansion Slots:

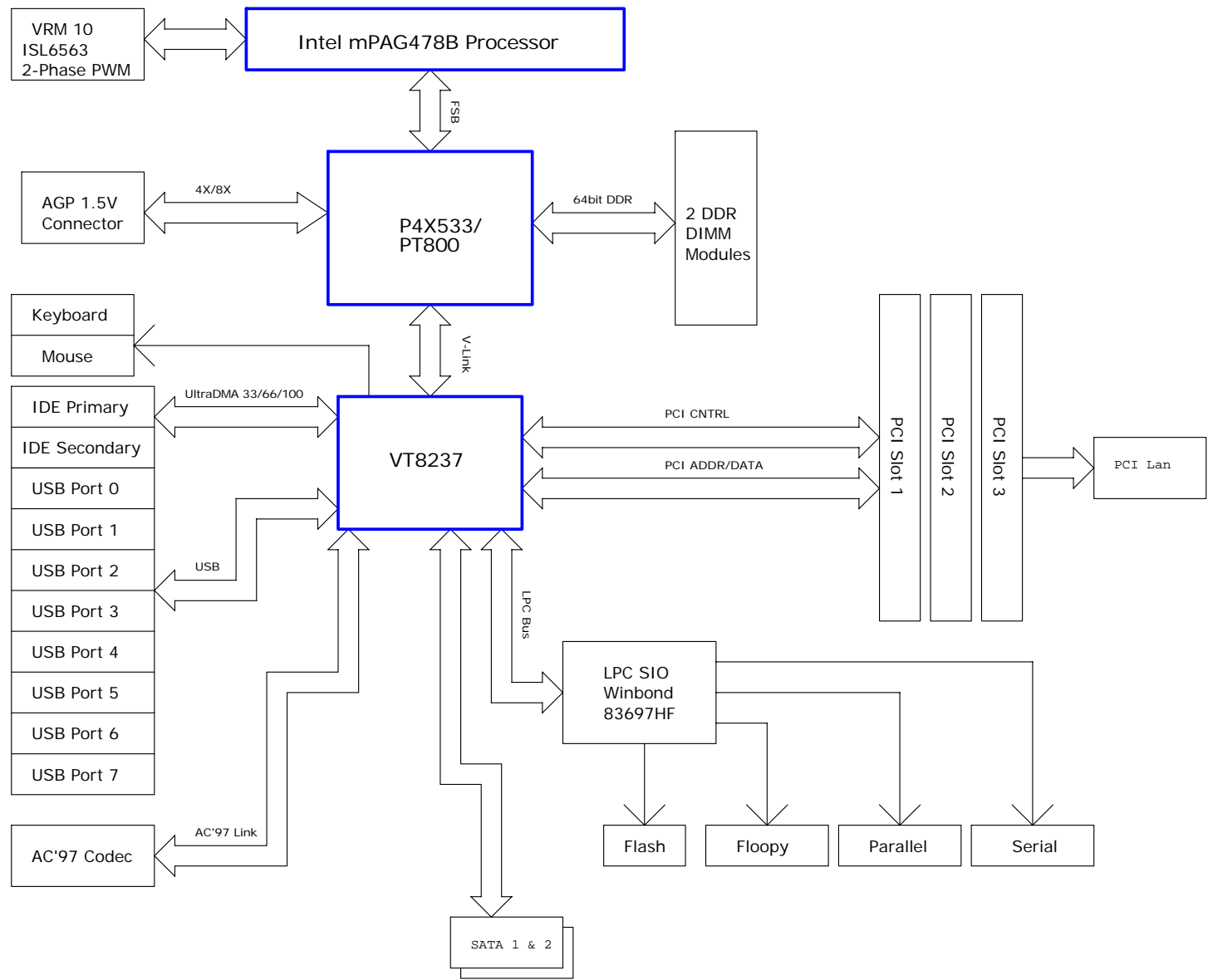
AGP * 1
PCI2.3 SLOT * 3

PWM:

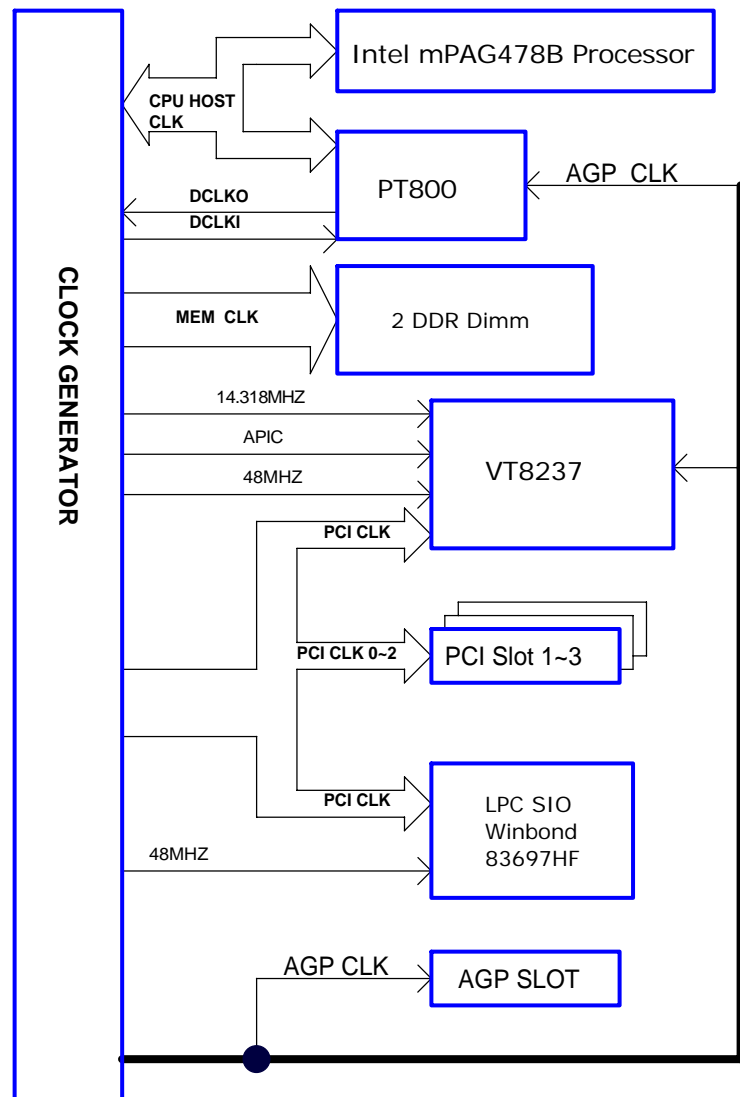
Controller: STL6710

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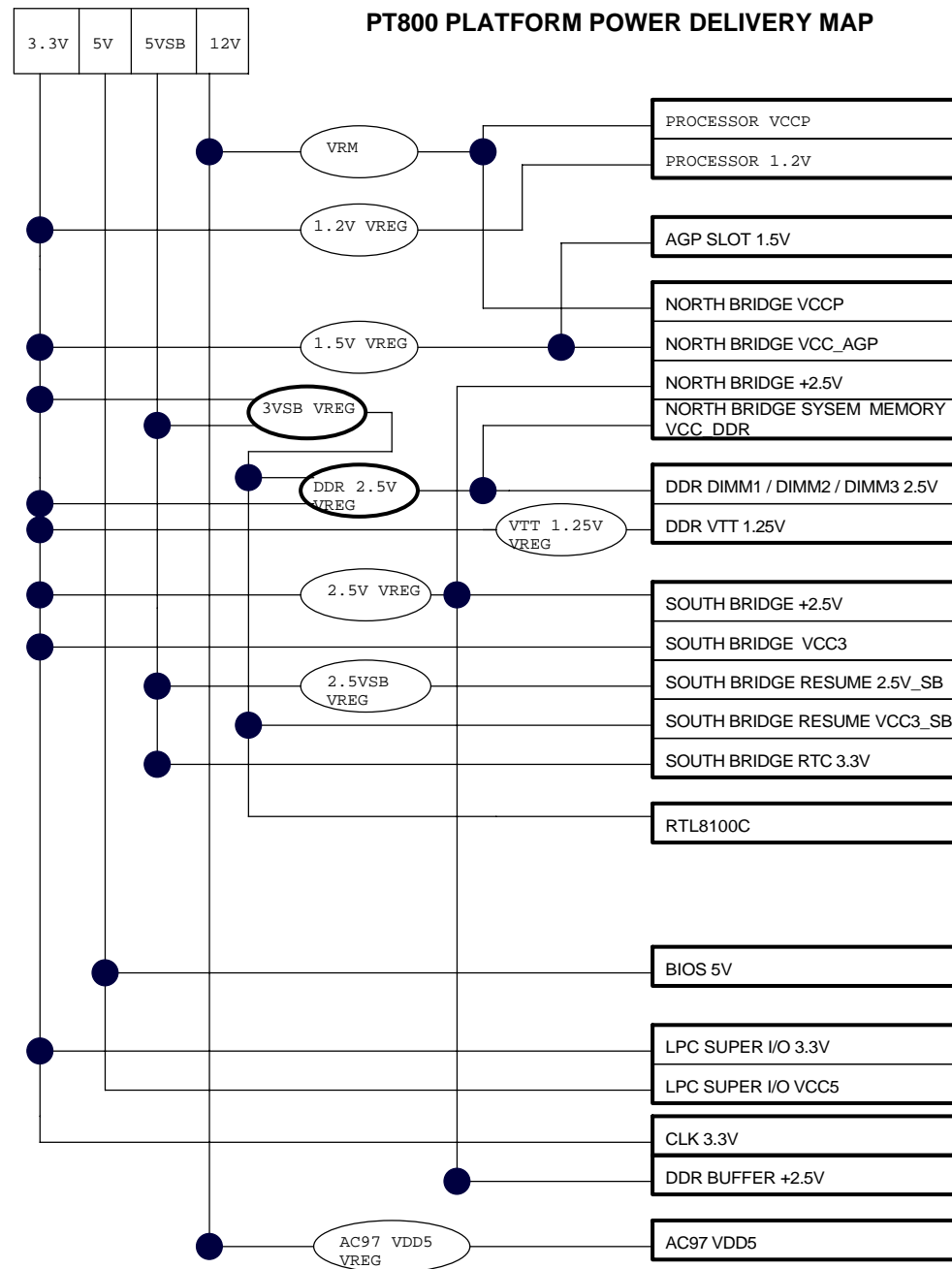
Block Diagram



PT800 PLATFORM CLOCK GENERATOR MAP



PT800 PLATFORM POWER DELIVERY MAP



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Title			
PWR AND CLOCK MAP			
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VT8237 GPIO Function Define

PIN NAME	Default Function	Function define	Pull up / down
GPO0 (VSUS33)	GPO0	NA	Pull up to 3VDUAL
GPO1 (VSUS33)	GPO1	NA	Pull up to 3VDUAL
GPO2/SUSA# (VSUS33)	SUSA#	SUSA#	
GPO3/SUSST1# (VSUS33)	SUSST1#	SUSST#	Pull up to 3VDUAL
GPO4/SUSCLK (VSUS33)	SUSCLK	SUSCLK	Pull up to 3VDUAL
GPO5/CPUSTP#	CPUSTP#	CPUSTP#	Pull up to VCC3
GPO6/PCISTP#	PCISTP#	PCISTP#	Pull up to VCC3
GPO7/GNT5	GP07	GNT5 NA	
GPO8/GPI8/VGATE	GPI8	VGATE NA	Pull up to VCC3
GPO9/GPI9/UDPWREN	GPI9	NA	
GPO10/GPI10/INTE#	GPI10	PIRQE# NA	Pull up to VCC
GPO11/GPI11/INTF#	GPI11	PIRQF# NA	Pull up to VCC
GPO12/GPI12/INTG#	GPI12	PIRQG# NA	Pull up to VCC
GPO13/GPI13/INTH#	GPI13	PIRQH# NA	Pull up to VCC
GPO14/GPI14/APICD0	GPI14	APICD0# NA	Pull up to VCC3
GPO15/GPI15/APICD1	GPI15	APICD1# NA	Pull up to VCC3
GPO20/GPI20/ACSDIN2	SDIN2	AC_SDIN2 NA	Pull down to GND
GPO21/GPI21/ACSDIN3	SDIN3	AC_SDIN3 NA	Pull down to GND
GPO22/GPI22/GHI#	GPI22	GHI# NA	Pull up to VCC3
GPO23/GPI23/DPSLP	GPI23	-LDTSTOP	Pull up to VCC3
GPO24/GPI24/GPIOA	GPIOA	LDT Freq Strapping bit1	Pull down to GND
GPO25/GPI25/GPIOB	GPIOB	LDT Width (L=8 bit,H=8 bit)	Pull down to GND
GPO26/GPI26/SMBDT2	SMBDT2	DETECT Chips H>PT800 L>P4X533	Pull up to 3VDUAL Pull down to GND
GPO27/GPI27/SMBCK2	SMBCK2	NA	
GPO28/GPI28/VIDSEL	GPI28	SATA_LED	Pull down to VCC5
GPO29/GPI29/VRDSLP	GPI29	VRDSLP NA	Pull down to GND
GPO30/GPI30/GPIOC	GPIOC	LDT Freq Strapping bit0	Pull down to GND
GPO31/GPI31/GPIOD	GPIOD	Fast Command (0:disable)	Pull down to GND
GPI0 (VBAT)	GPI0	GPI0 NA	Pull up to VBAT
GPI1 (VSUS33)	GPI1	ATADET0=>Detect IDE1 ATA100/66	Pull up to 3VDUAL
GPI2/EXTSMI# (VSUS33)	EXTSMI#	EXTSMI#	Pull up to 3VDUAL
GPI3/RING# (VSUS33)	RING#	RING#	Pull up to 3VDUAL
GPI4/LID# (VSUS33)	LID#	ATADET1=>Detect IDE2 ATA100/66	Pull up to 3VDUAL

PCI RESET DEVICE

Signals	Target
PCIRST#1	NB,LAN,I/O
PCIRST#2	PCI slot 1-3
HD_RST#	Primary, Scondary IDE

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD16	PCICLK0	15 (PCI_CLK4)
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD17	PCICLK1	17 (PCI_CLK5)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD18	PCICLK2	18 (PCI_CLK6)
PCI_LAN	INTD#	PCI_REQ#3 PCI_GNT#3	AD19	LAN_CLK	14 (PCI_CLK3)

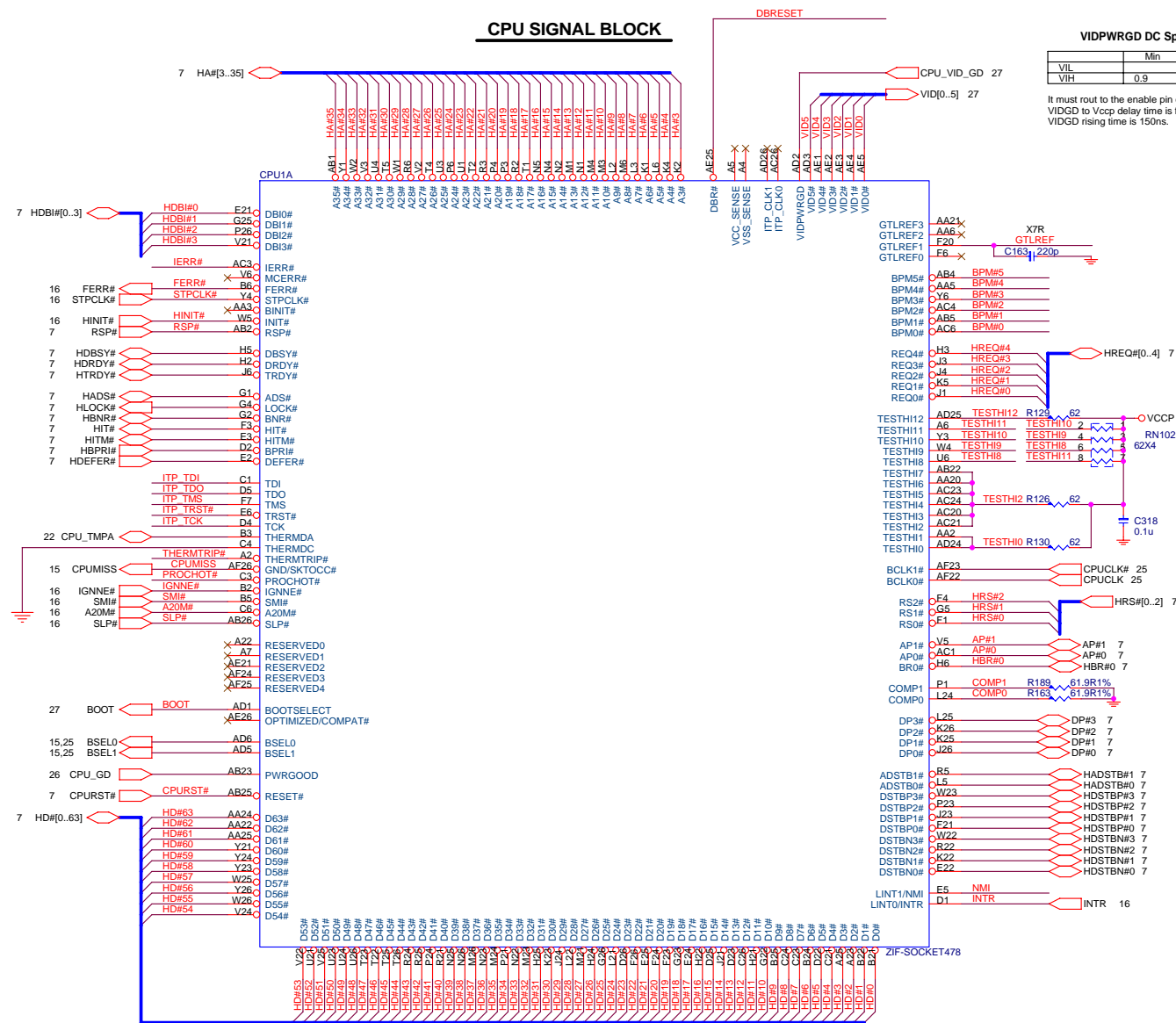
PIN NAME	Default Function	Function define	Pull up / down
GPI5/BATLOW# (VSUS33)	BATLOW#	BATLOW# NA	Pull up to 3VDUAL
GPI6/AGPBZ	AGPBZ	AGPBZ# NA	Pull up to VCC3
GPI7/REQ5	GPI7	PREQ#5 NA	Pull up to VCC3
GPI16/INTRUDER# (VBAT)	INTRUDER#	INTRUDER NA	Pull up to VBAT
GPI17/CPUMISS	CPUMISS	CPUMISS NA	Pull up to 3VDUAL
GPI18/AOLGPI1/THRM#	AOLGP1	THRM#	Pull up to VCC3
GPI19/APICCLK	APICCLK	APICCLK NA	
8237 Strapping	State	Function define	Pull up / down
VT8237>>PDA0	Low	LDT Transmit timing control 1/0 : enable / disable	Pull down to GND
VT8237>>PDA1	Low	External loop test mode 1/0 : enable / disable	Pull down to GND
VT8237>>PDCS#3	Low	Test mode 1/0 : enable / disable	Pull down to GND
VT8237>>ACSDO	Low	Auto reboot 0/1 : enable / disable	Pull down to GND
VT8237>>PDA2	High	Romsip Select 1/0 : enable / disable	Pull up to VCC3
VT8237>>MII_EEDI	Low	Eliminate Lan 1/0:enable/disable	Pull down to VCC3
VT8237>>PDCS#1	High	SATA master/slave mode 0/1 : enable / disable	Pull up to VCC3
VT8237>>PDDACK#	High	External Sata Phy 0/1 : enable / disable	Pull up to VCC3
VT8237>>SPKR	High	CPU Freq Strapping 0/1 : enable / disable	Pull up to VCC3
VT8237>>ACSYNC	High	LPC FWH Command 0/1 : enable / disable	Pull up to VCC3

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MCLK0/MCLK#0 MCLK1/MCLK#1 MCLK2/MCLK#2
DIMM 2	1010001B	MCLK3/MCLK#3 MCLK4/MCLK#4 MCLK5/MCLK#5

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Title General Purpose Spec		
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CPU SIGNAL BLOCK

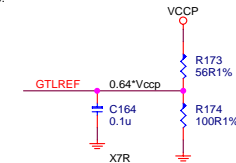


VIDPWRGD DC Specifications

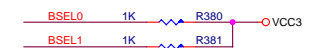
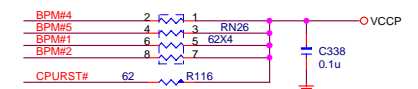
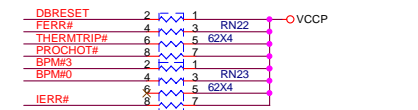
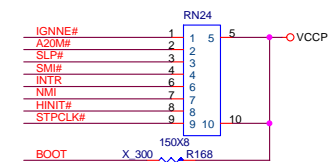
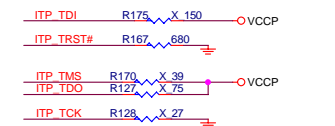
	Min	Typ	Max
V _{IL}			0.3
V _{IH}	0.9		

It must route to the enable pin of PWM and CK-409
VIDGD to Vccp delay time is from 1ms to 10ms.
VIDGD rising time is 150ns.

CPU GTL REFERENCE VOLTAGE BLOCK



CPU ITP BLOCK

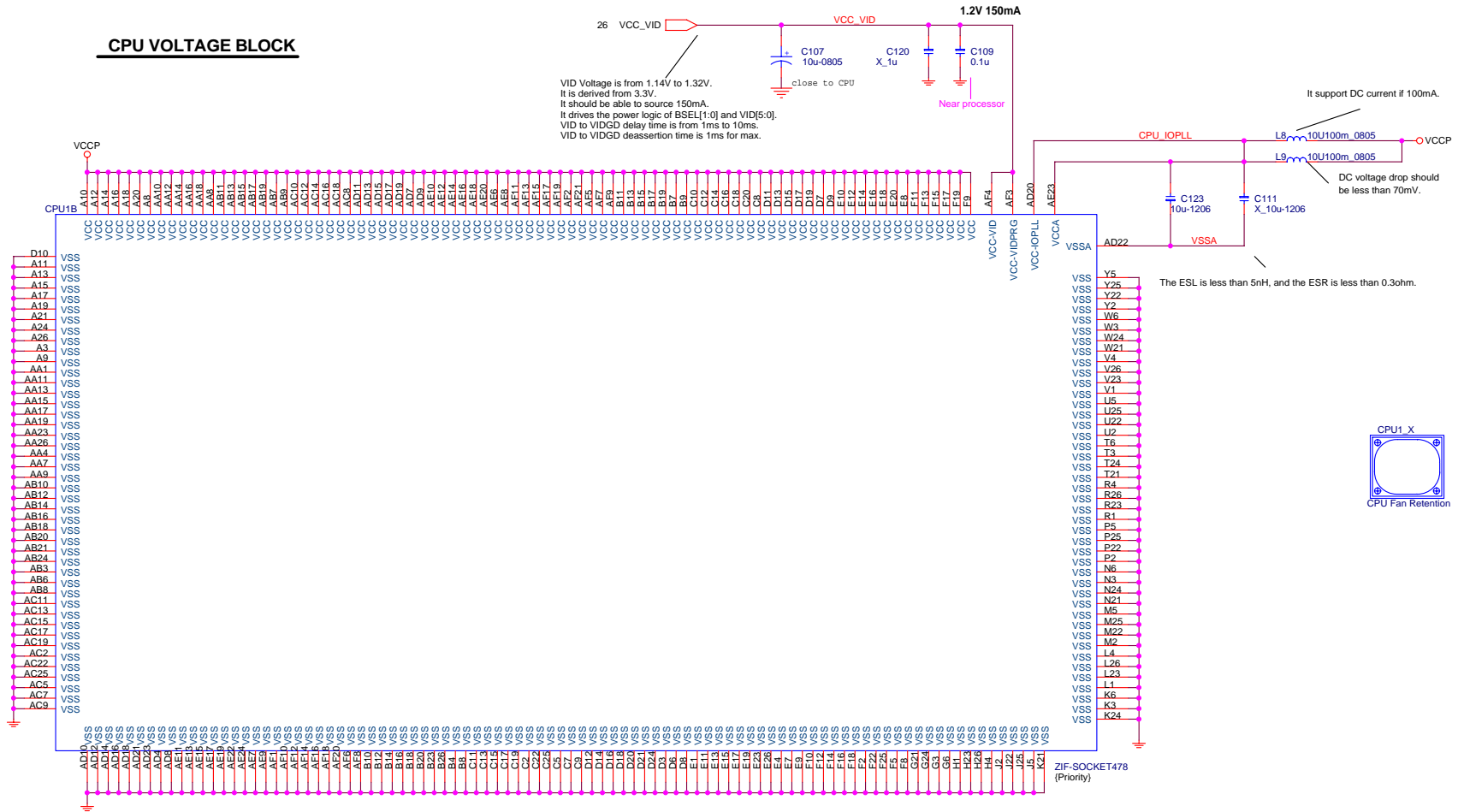


CPU STRAPPING RESISTORS

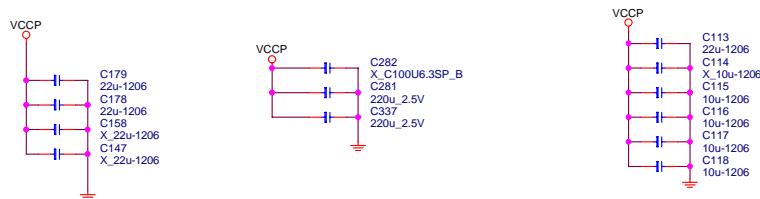
ALL COMPONENTS CLOSE TO CPU



CPU VOLTAGE BLOCK

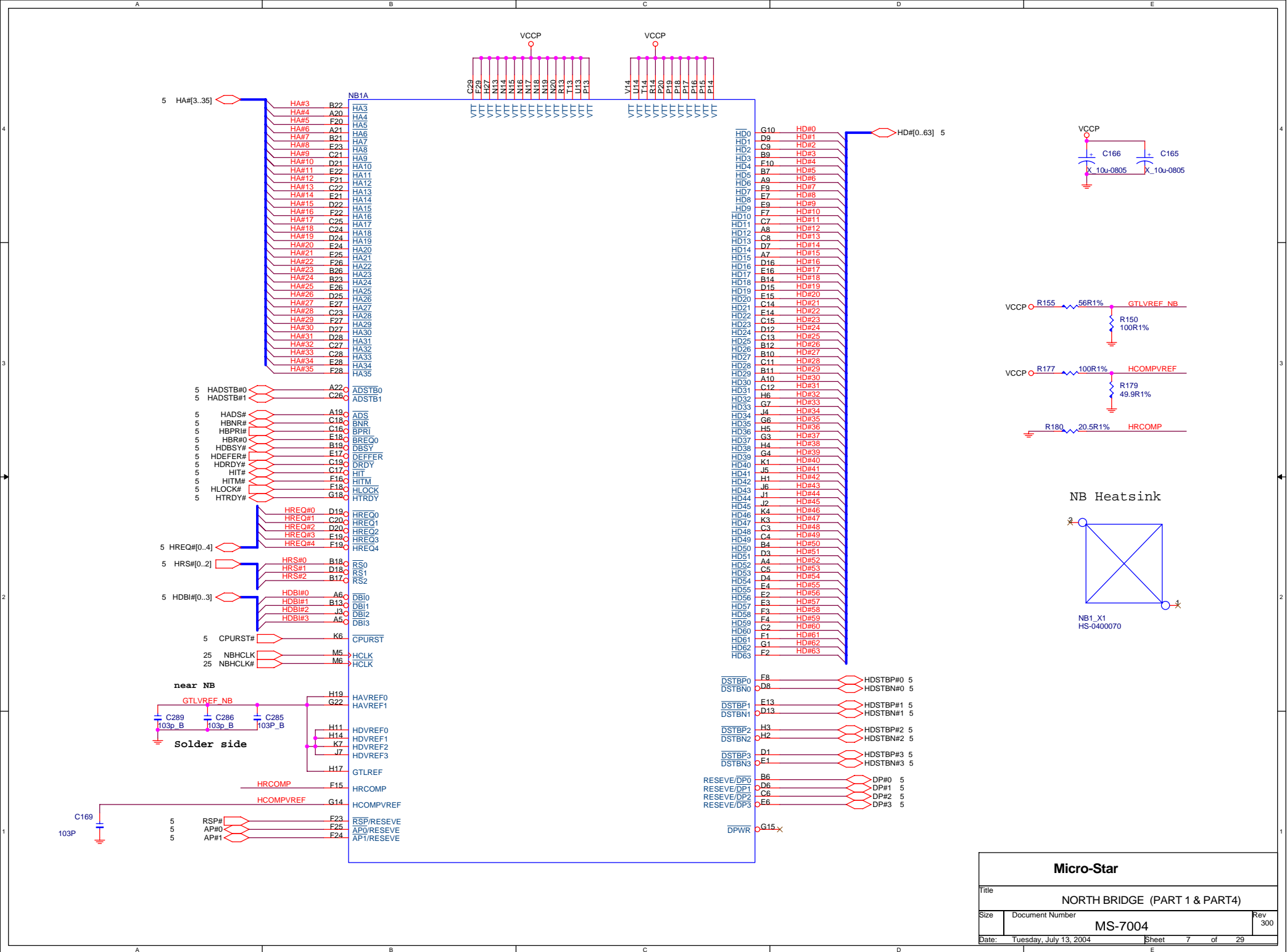


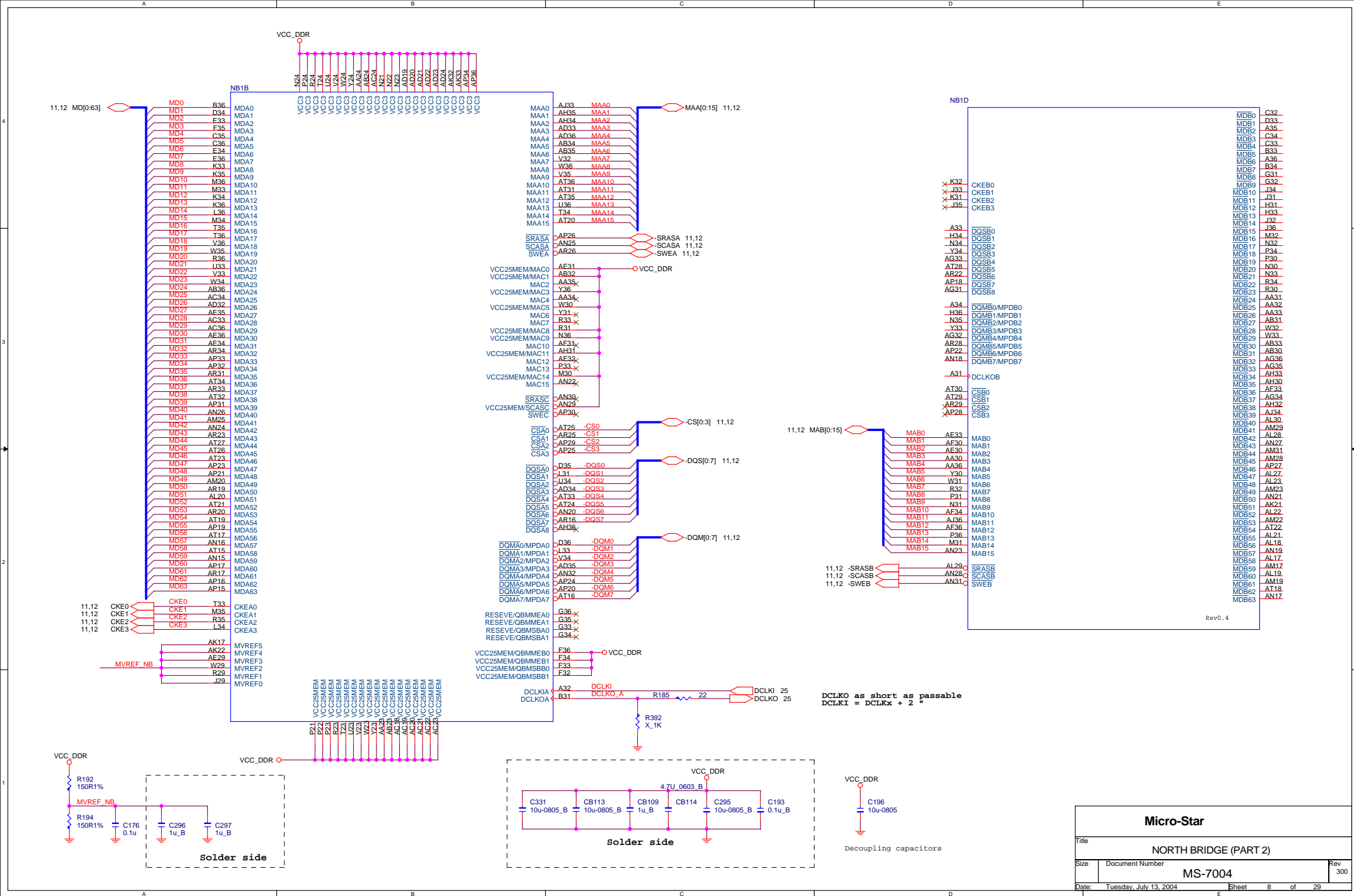
CPU DECOUPLING CAPACITORS

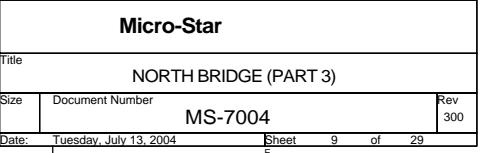


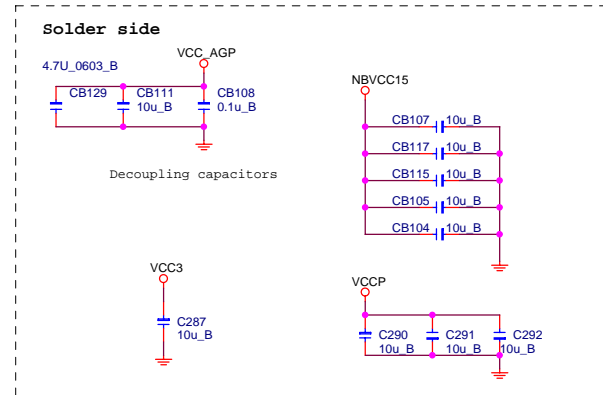
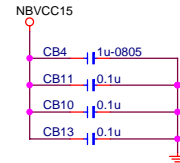
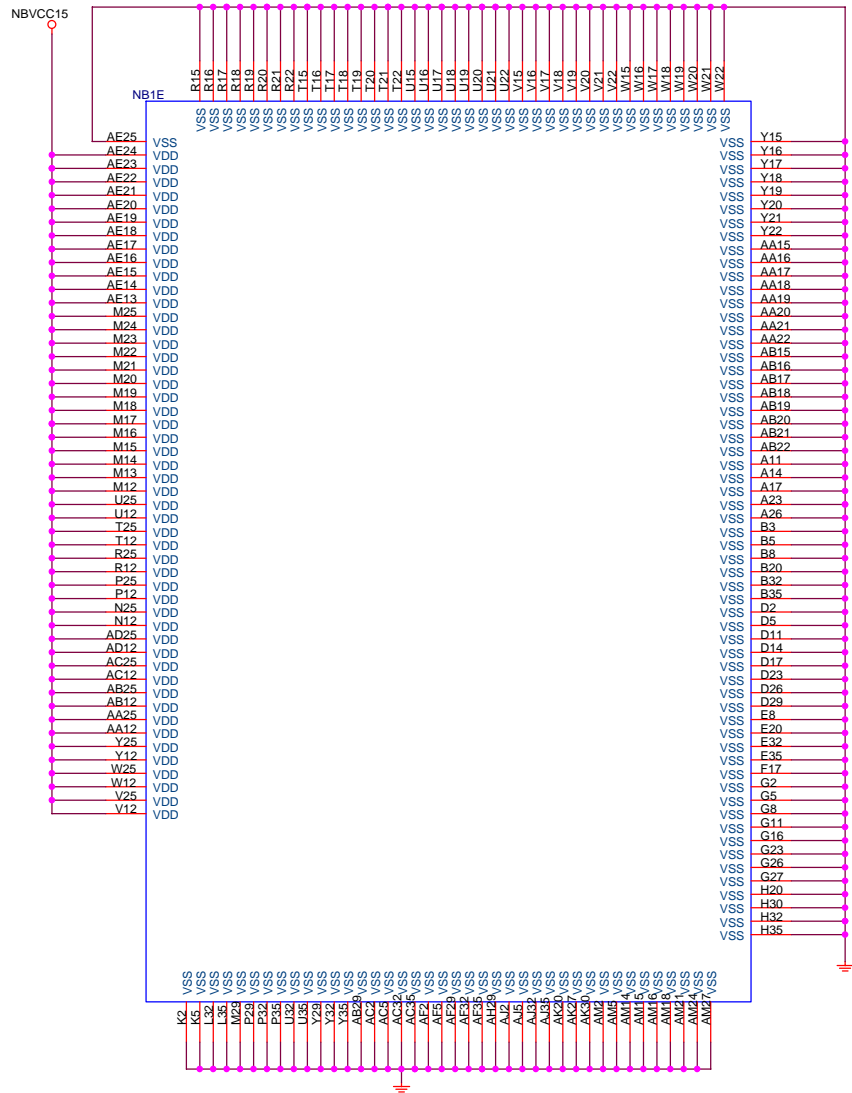
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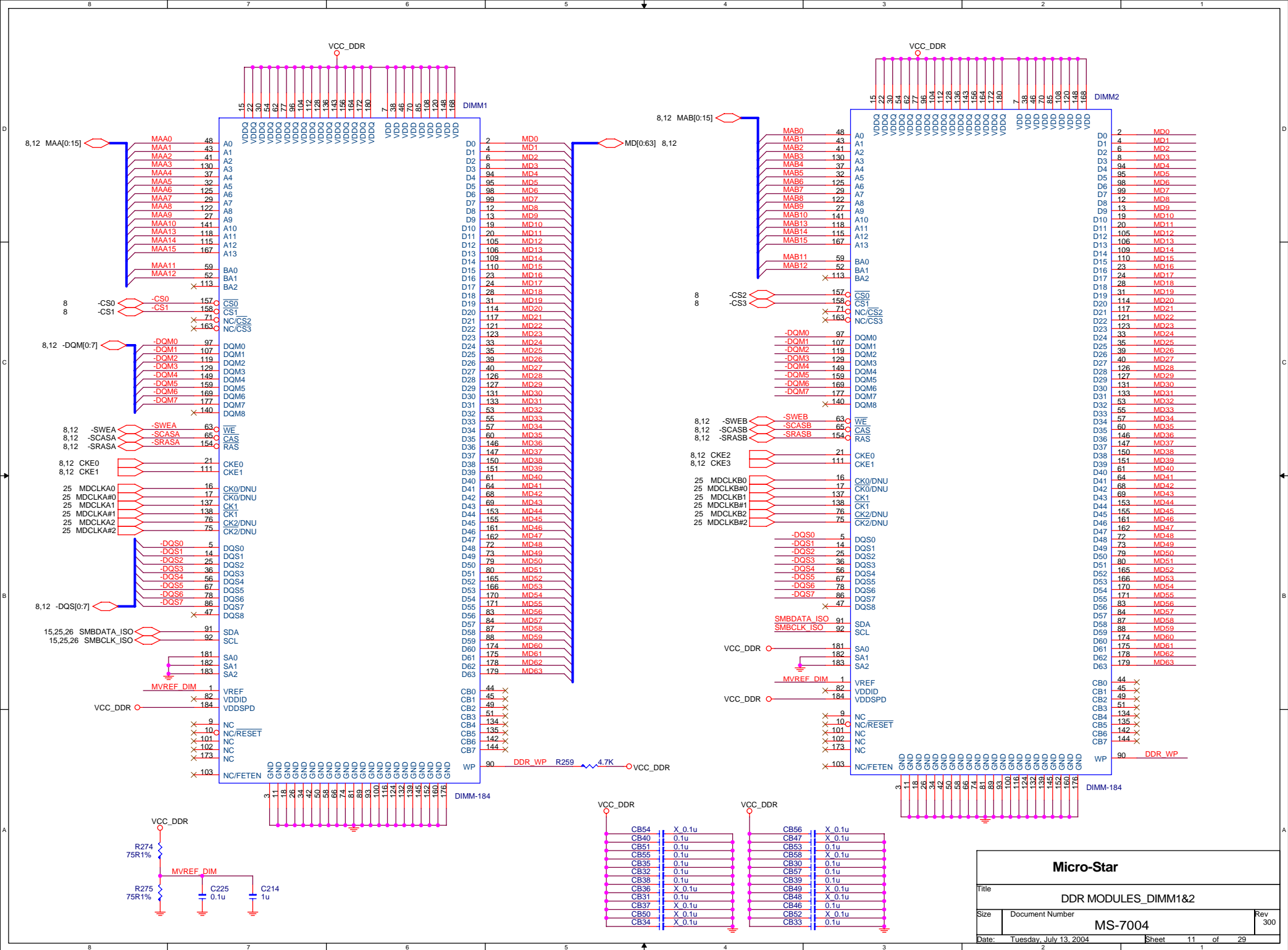


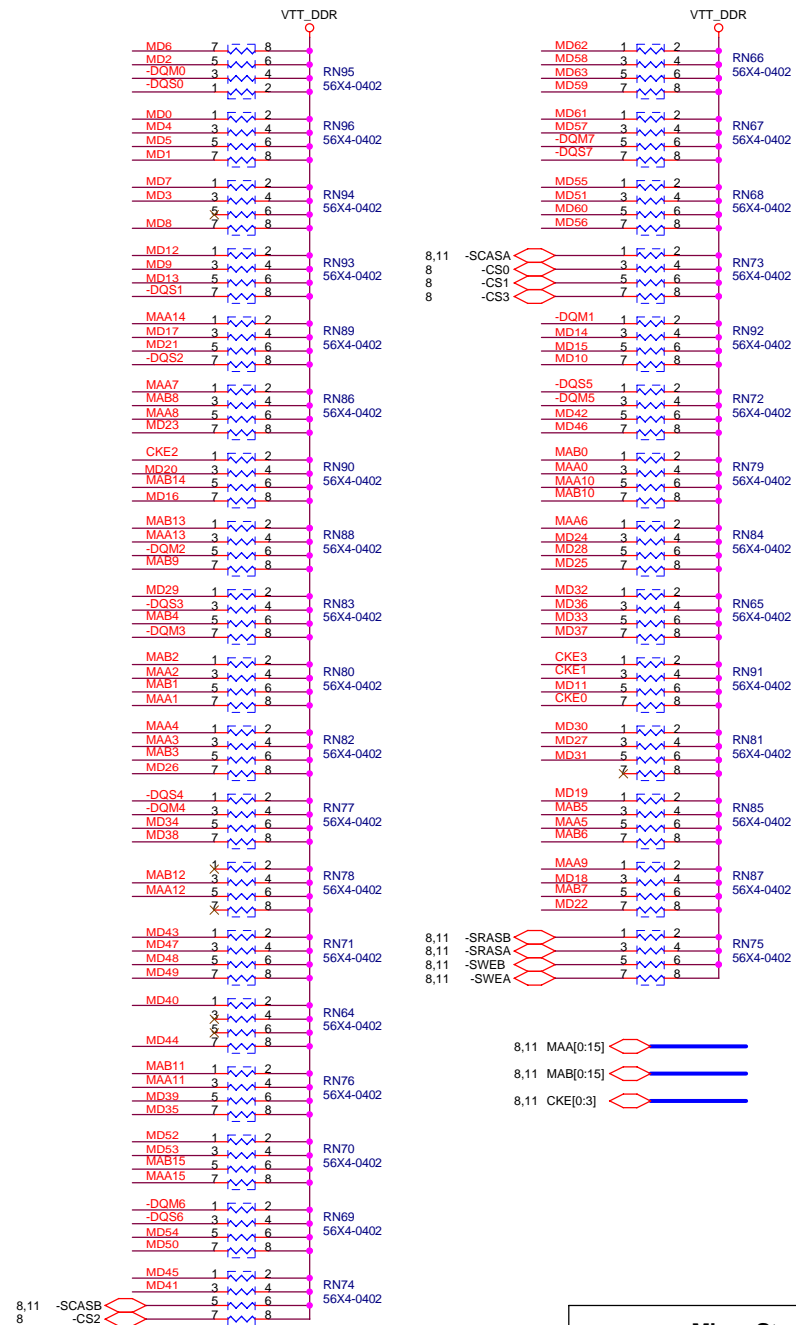
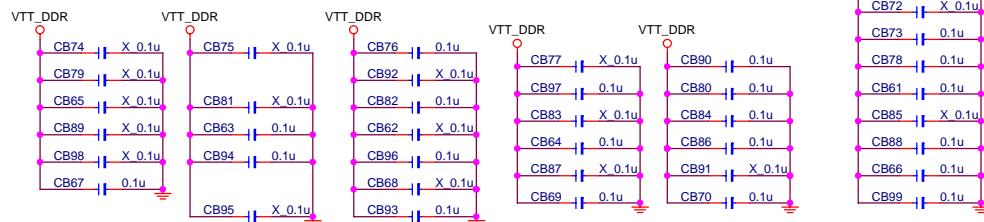
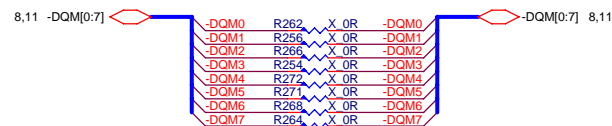
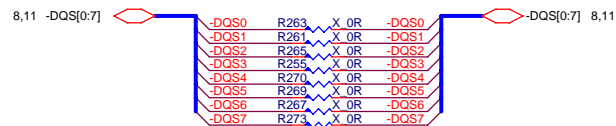


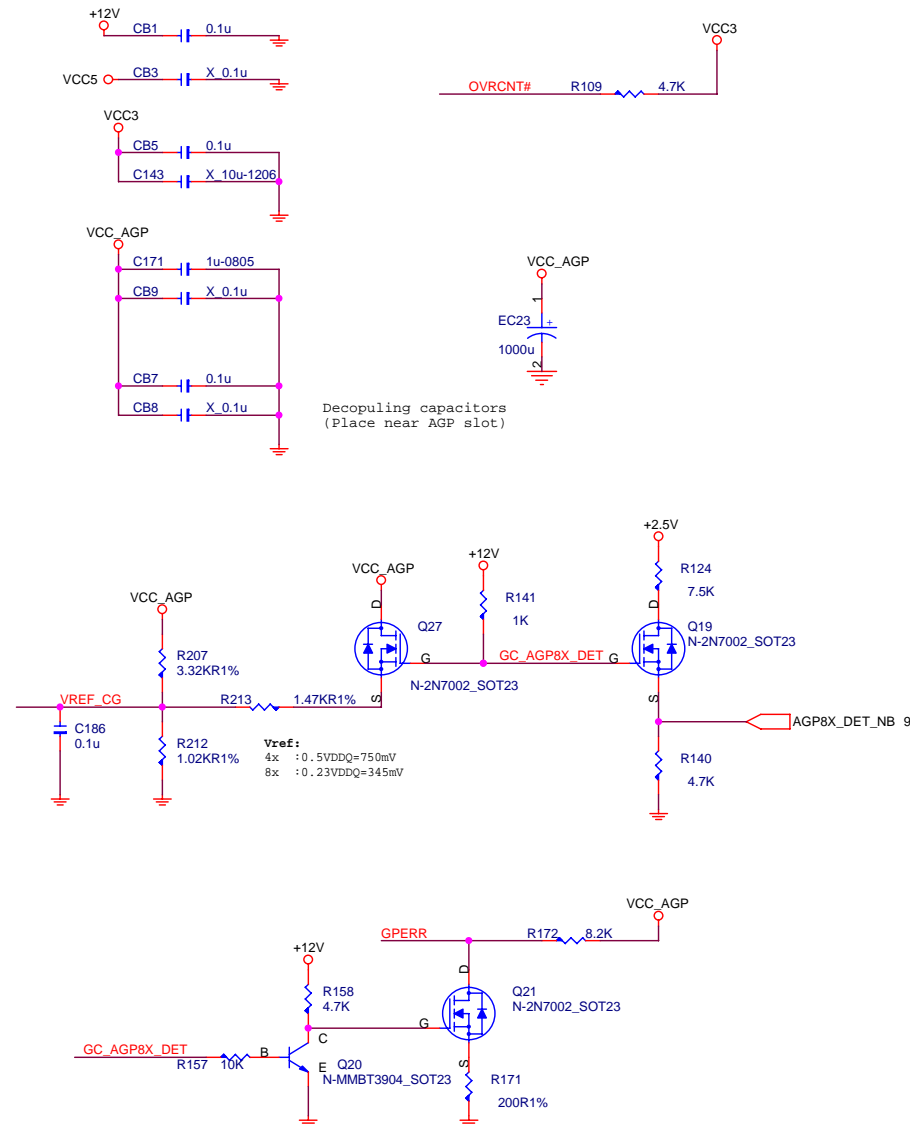
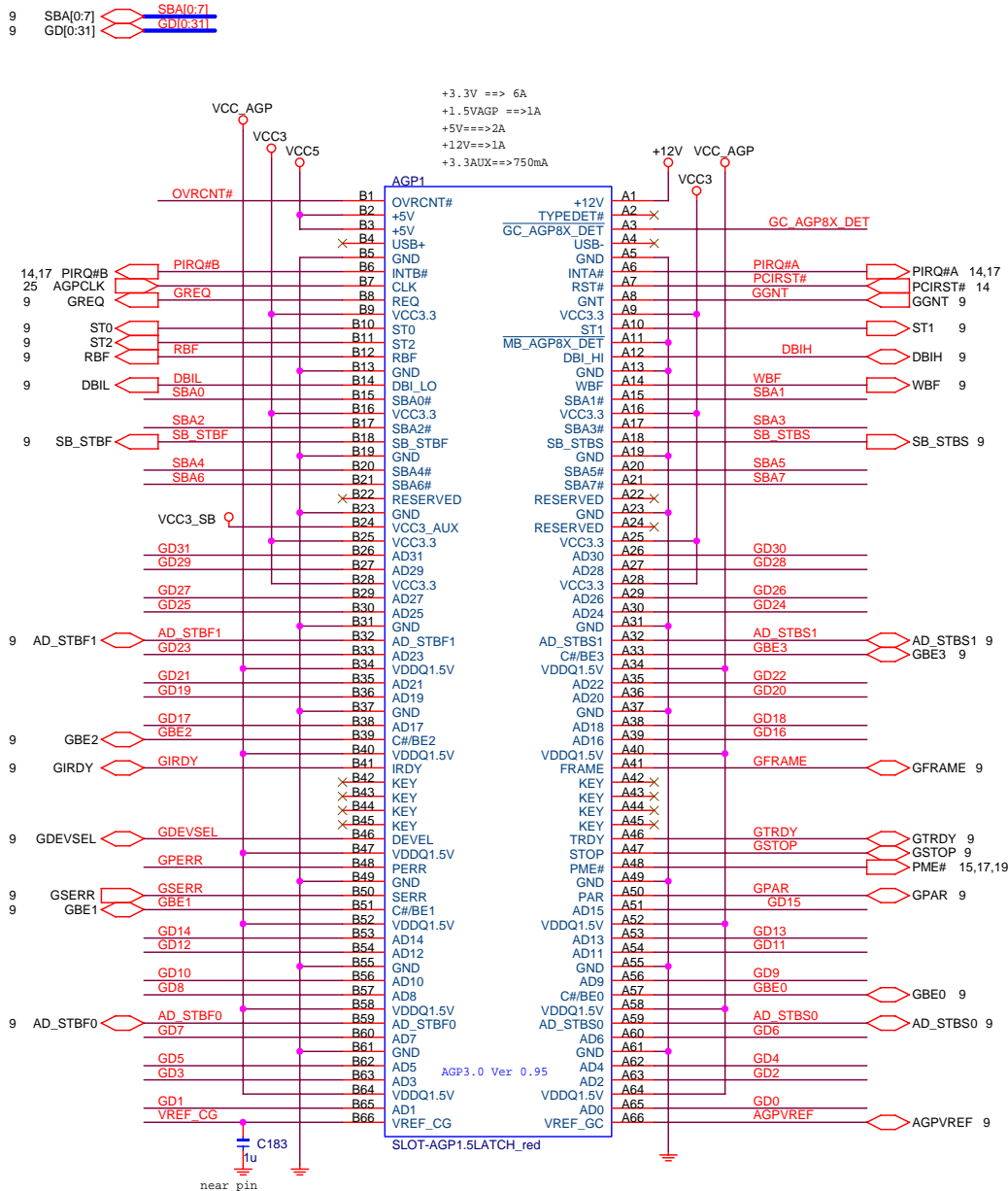




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NORTH BRIDGE (PART4)			
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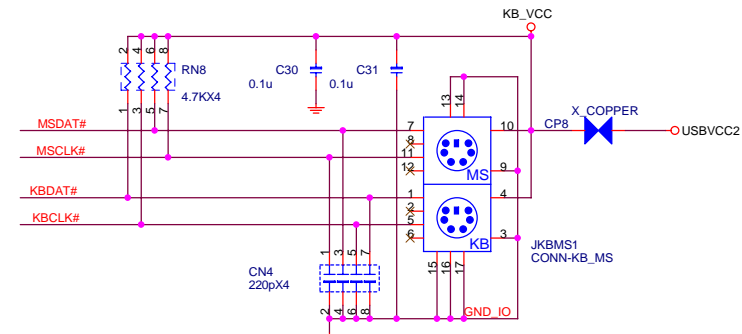
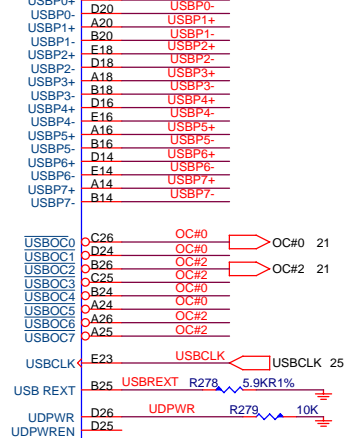
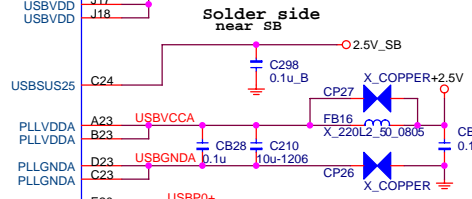
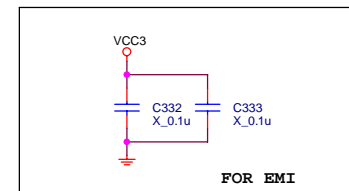
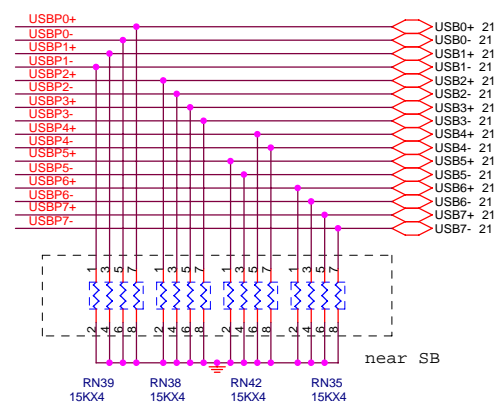
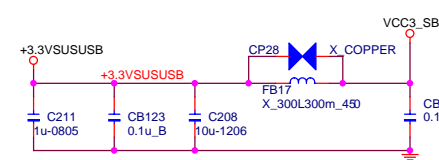
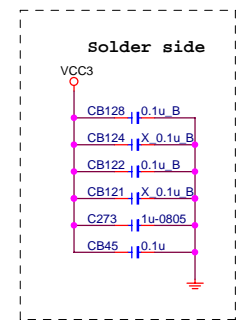
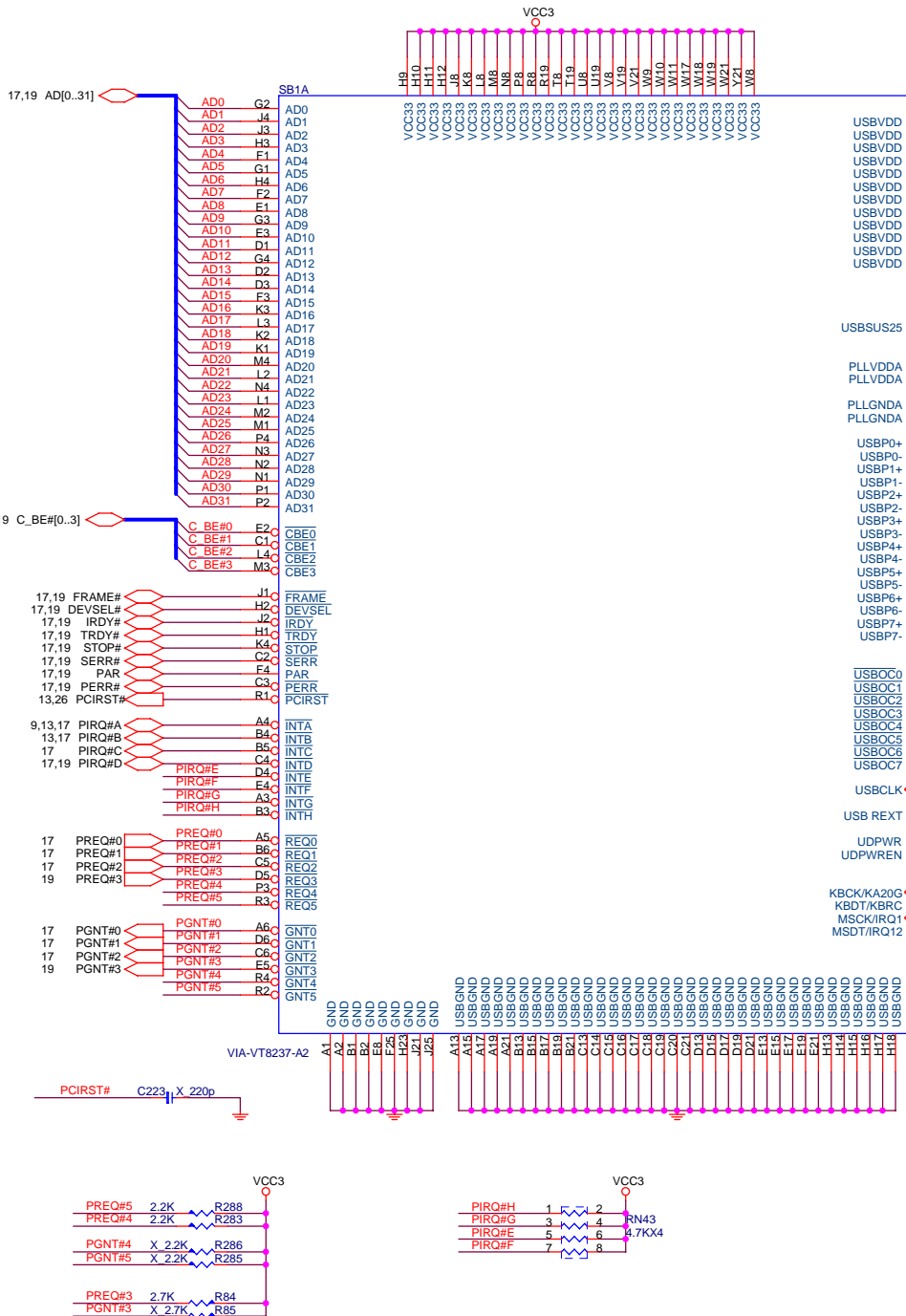




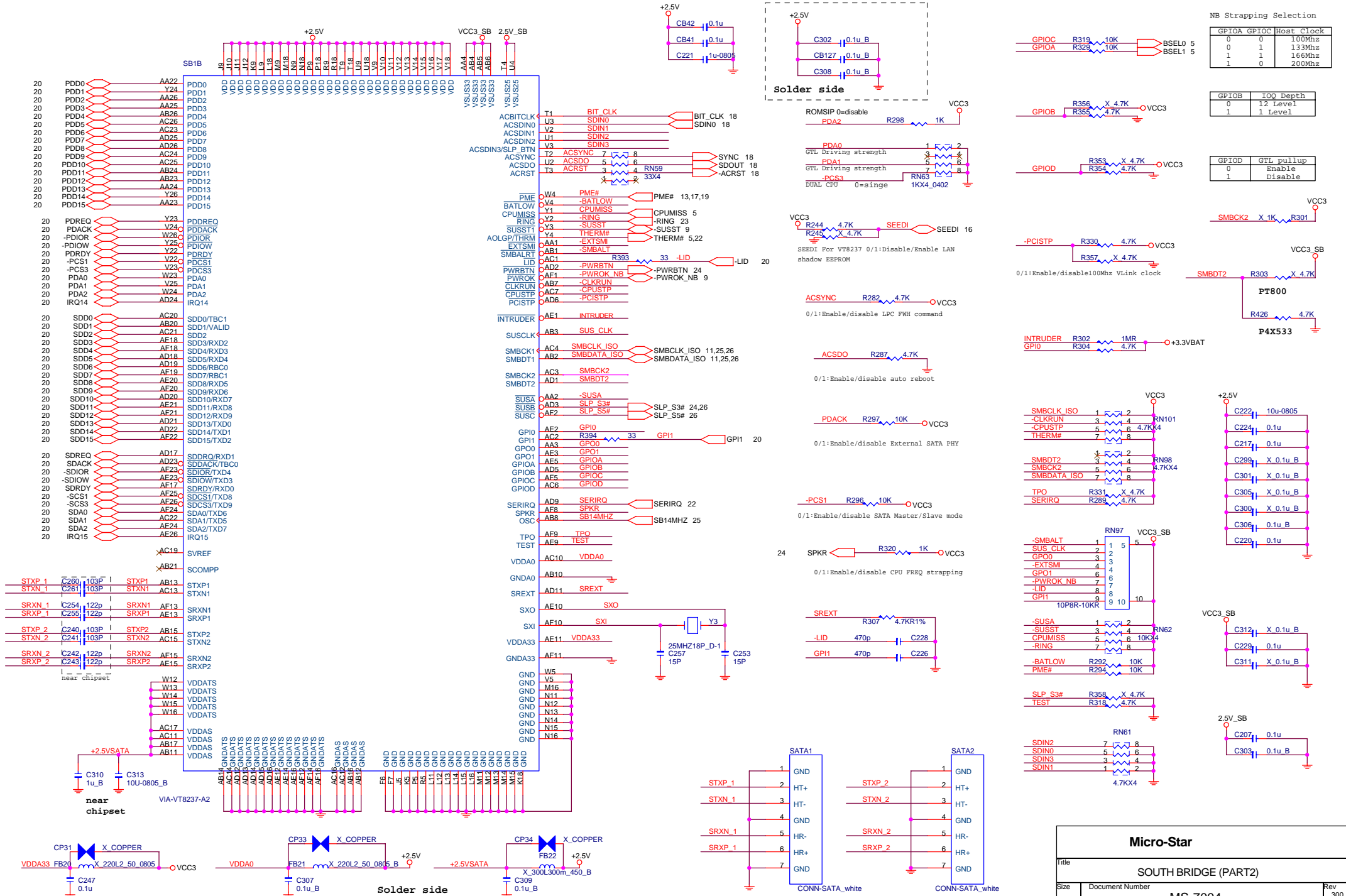


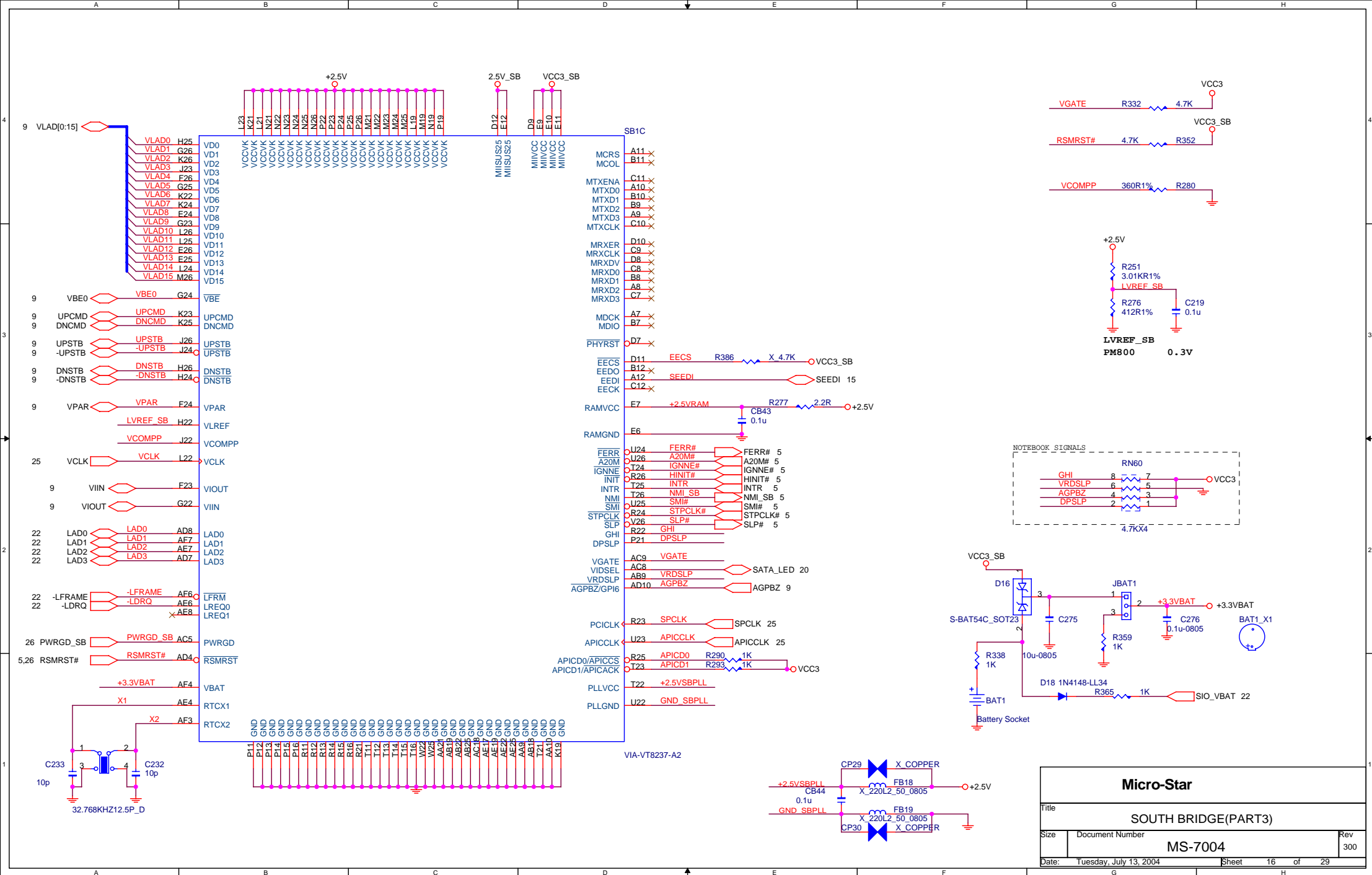
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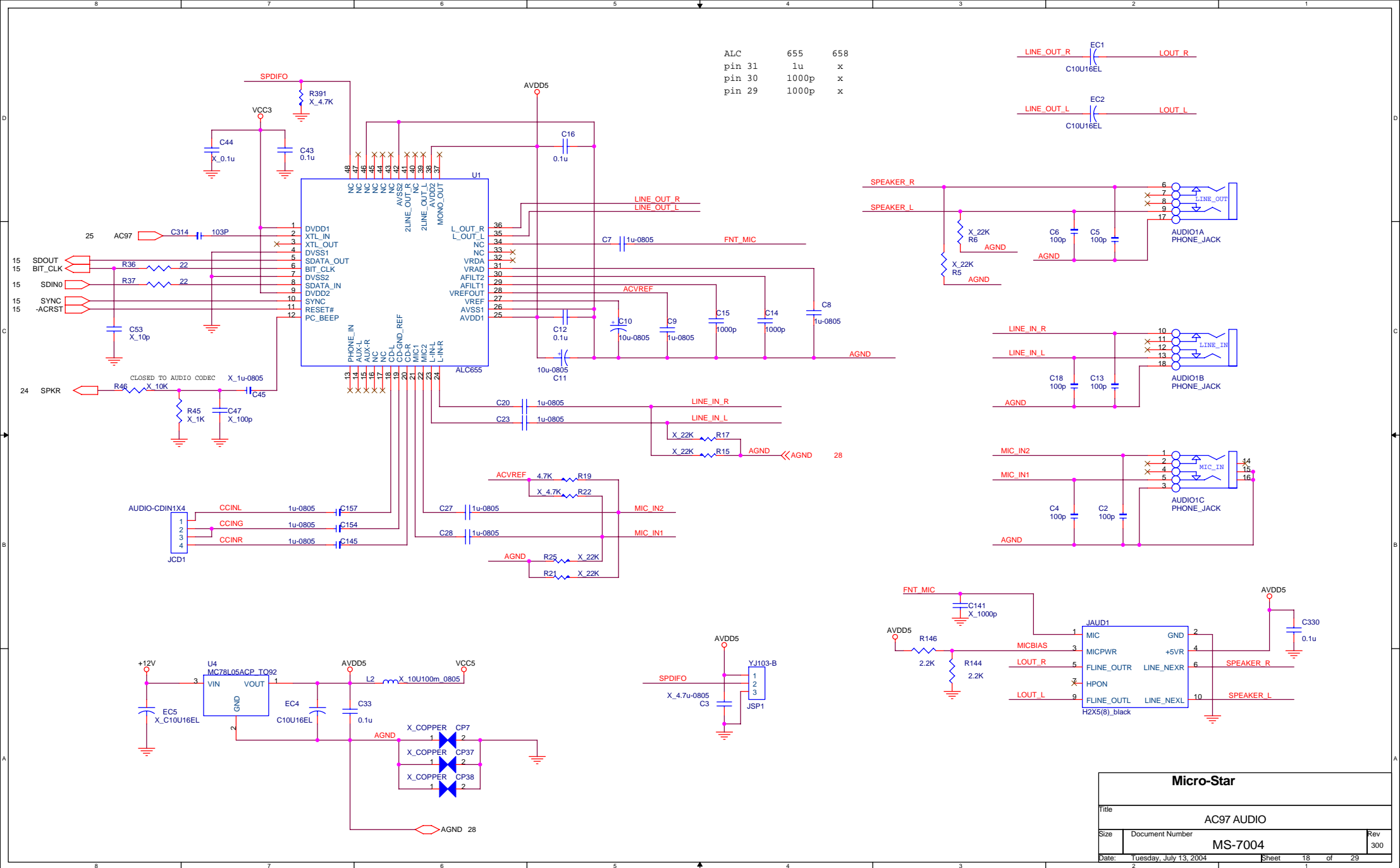
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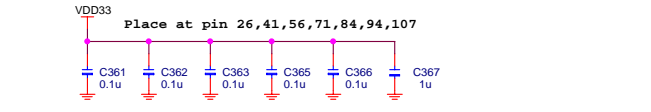
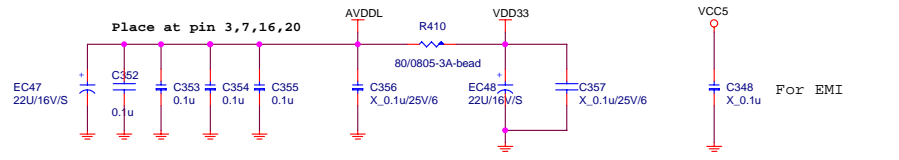
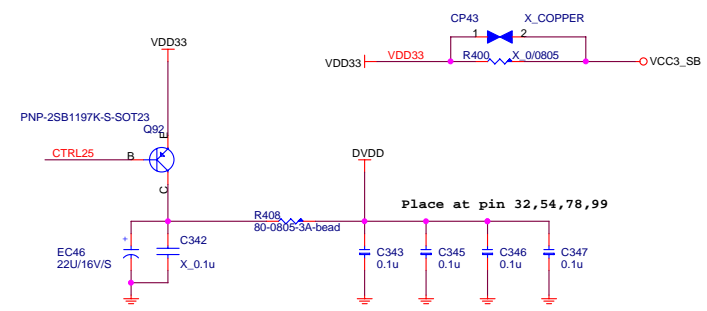
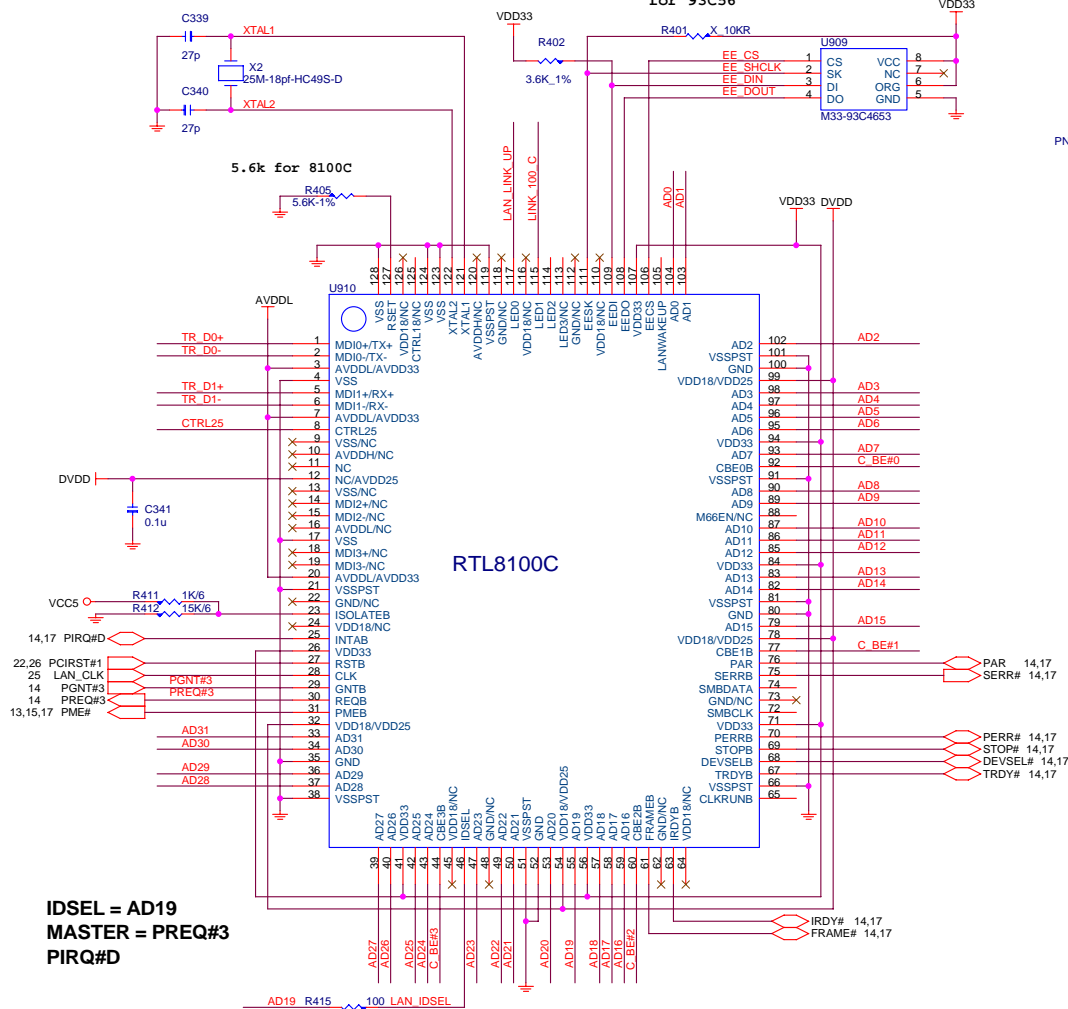
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SOUTH BRIDGE (PART1)			
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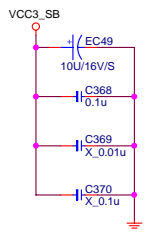




Stuff 10K for 93C56

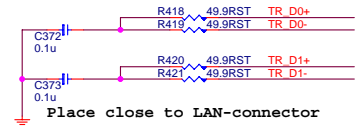


	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8100C	2.5V	2.5V	3.3V	X	2.5V

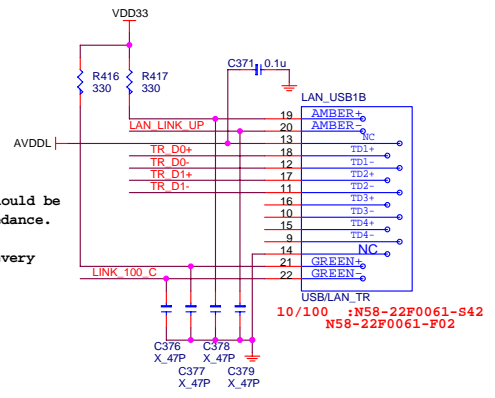


IDSEL = AD19
MASTER = PREQ#3
PIRQ#D

Place close to LAN-chip.



1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.

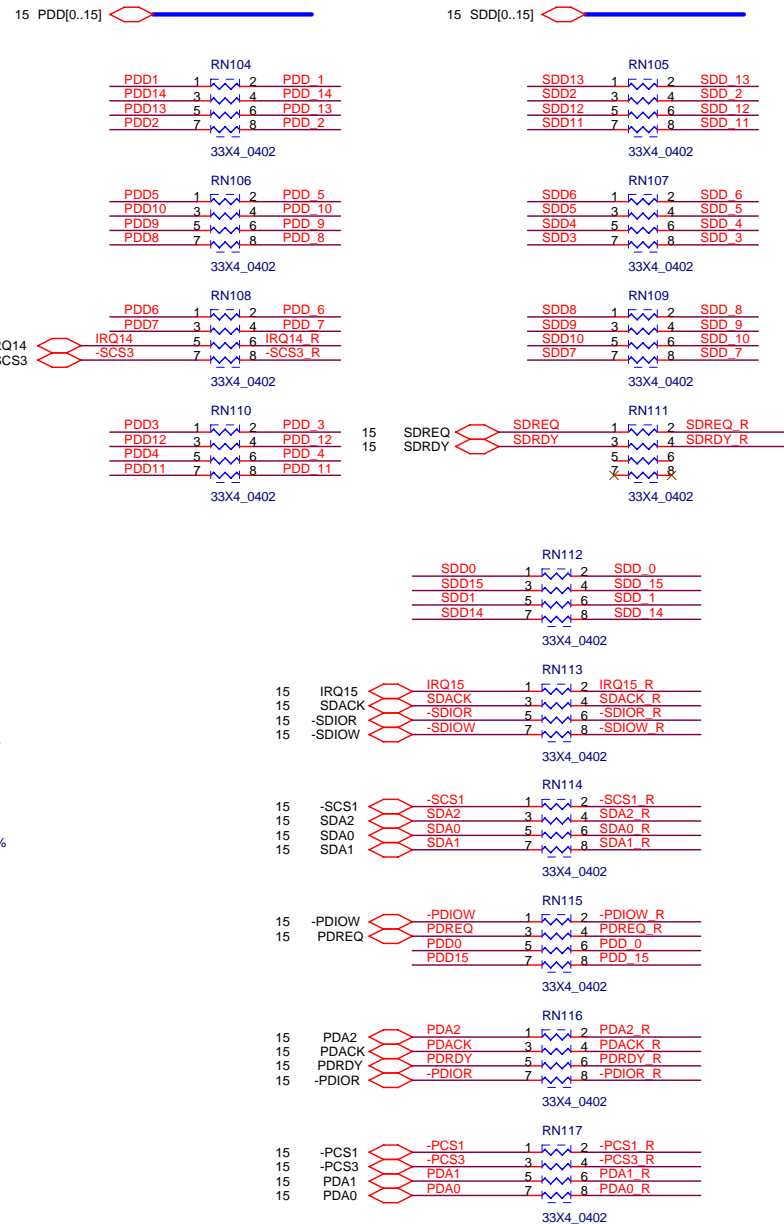
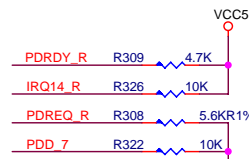
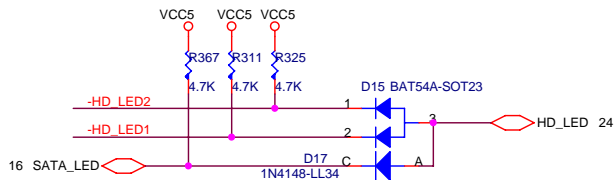
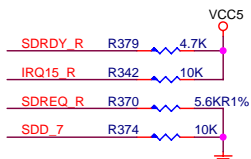
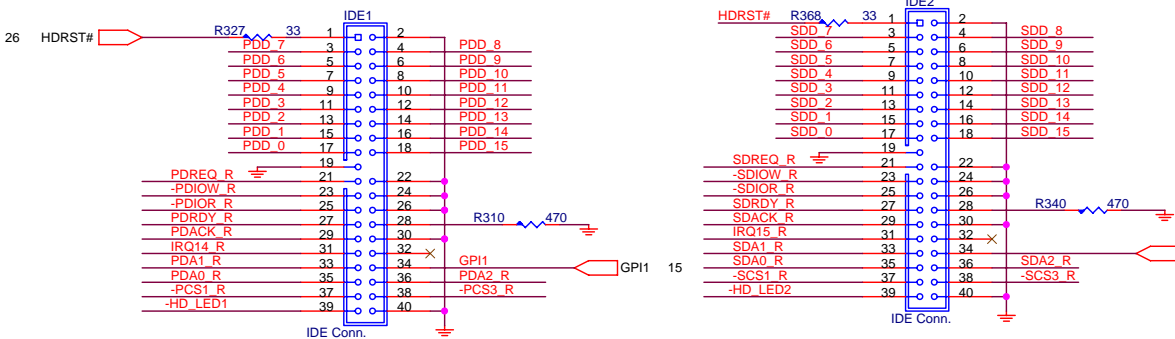


Reserved for EMI.

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LAN_RTL8100C		
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PRIMARY

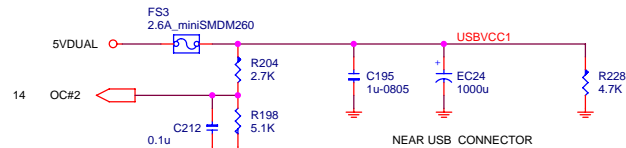
SECONDARY



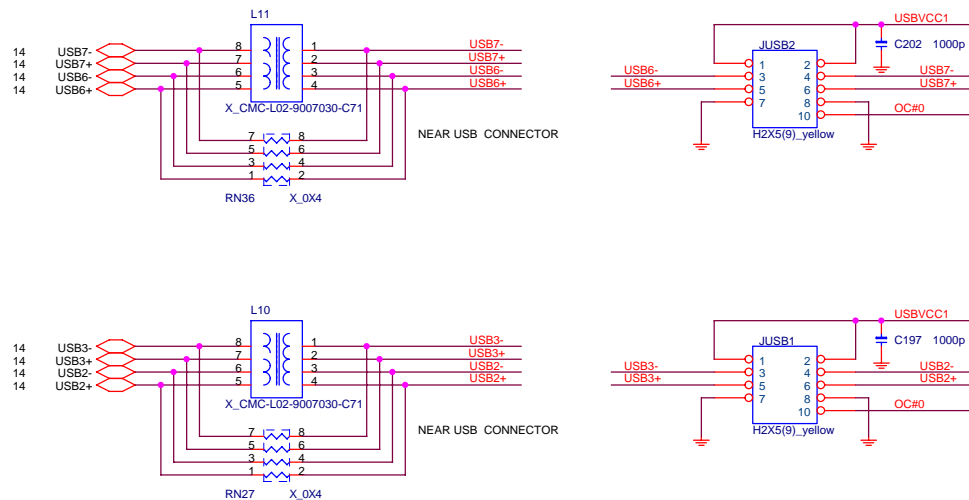
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IDE CONNECTORSSize
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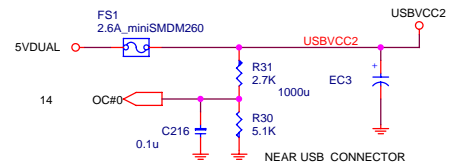
POWER CIRCUIT FOR USB PORT 4,5,6,7



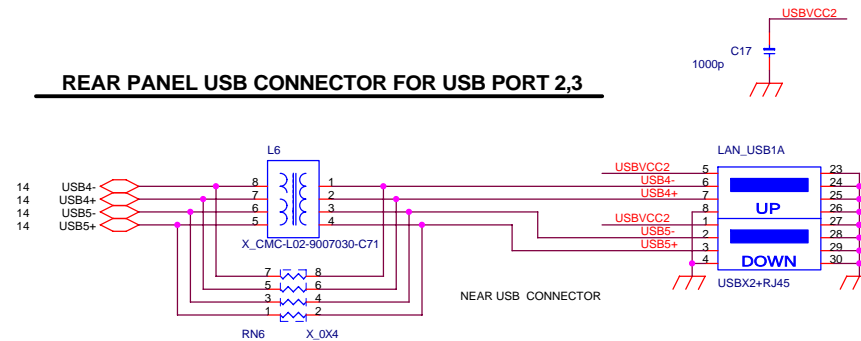
REAR PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



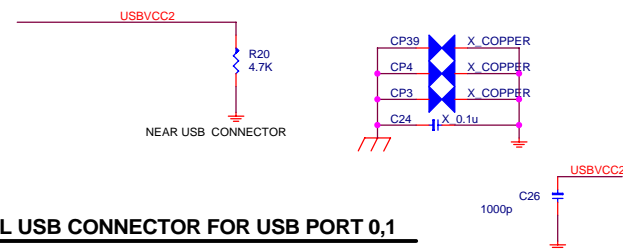
POWER CIRCUIT FOR USB PORT 2,3



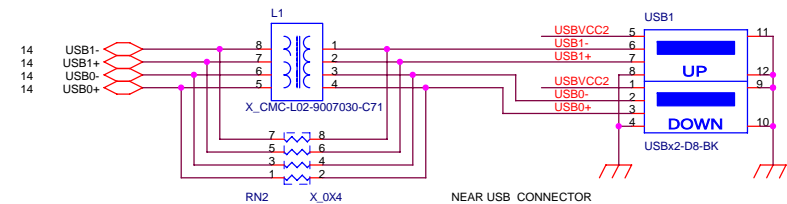
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POWER CIRCUIT FOR USB PORT 0,1



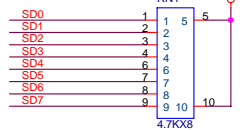
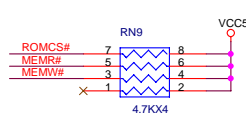
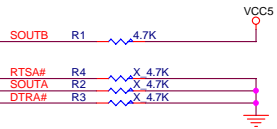
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



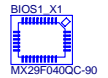
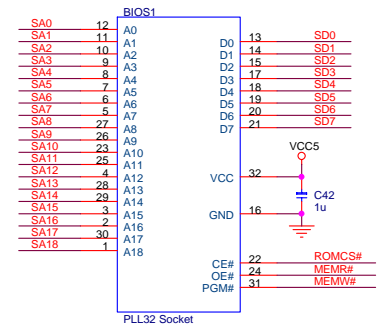
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USB Connectors		
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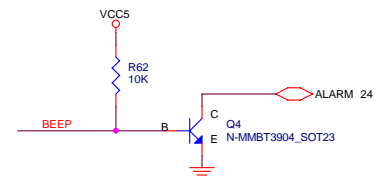
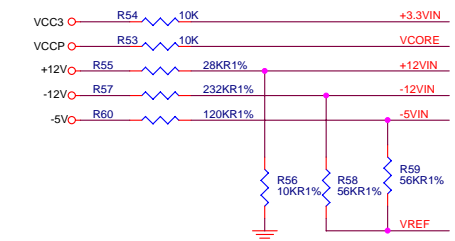
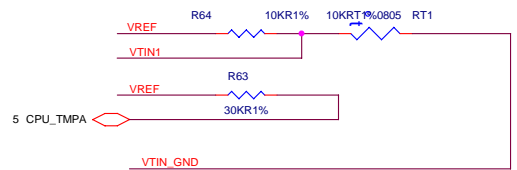
STRAPS

RTSA# L: CFAD=2E H: CFAD=4E
SOUTB L: 24MHZ

Flash Rom



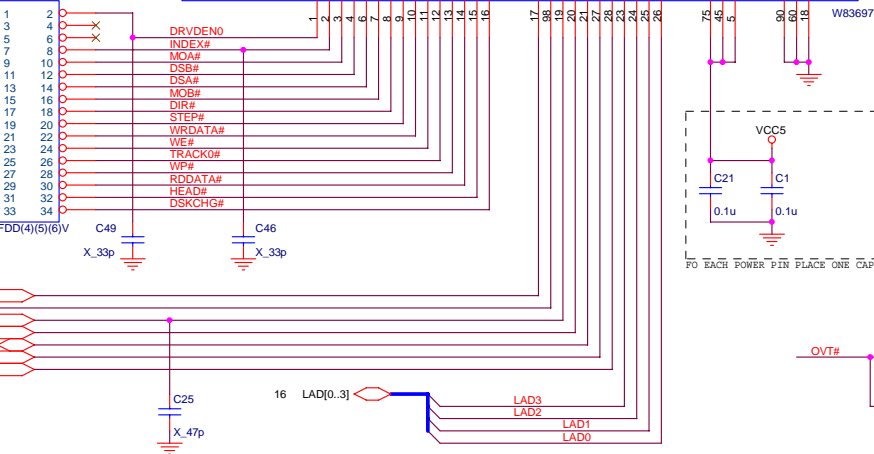
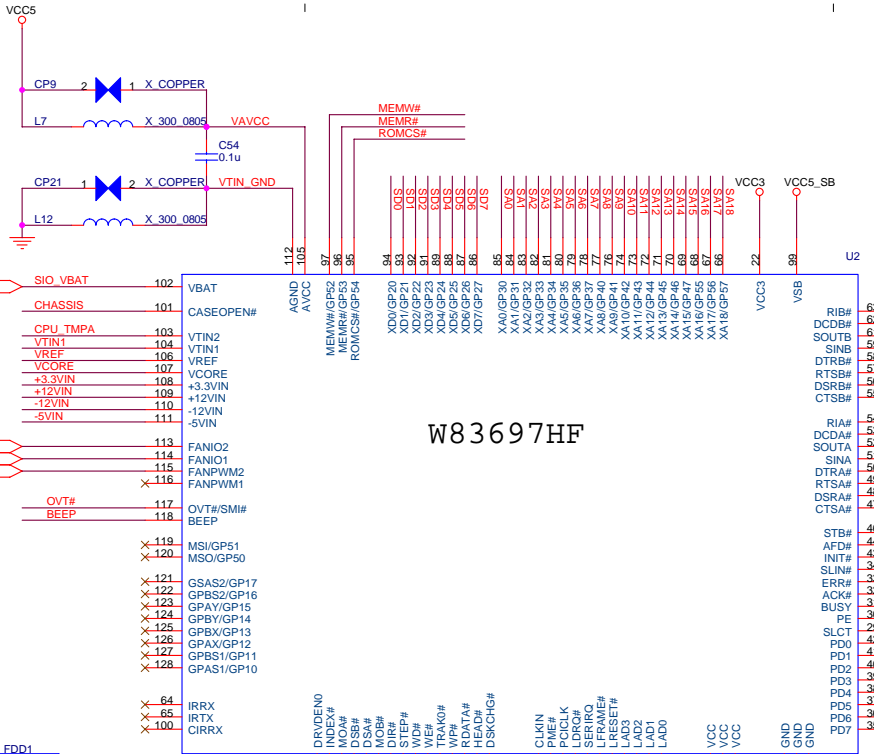
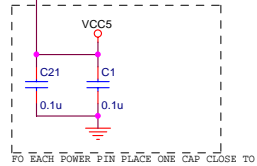
Hardware Monitor



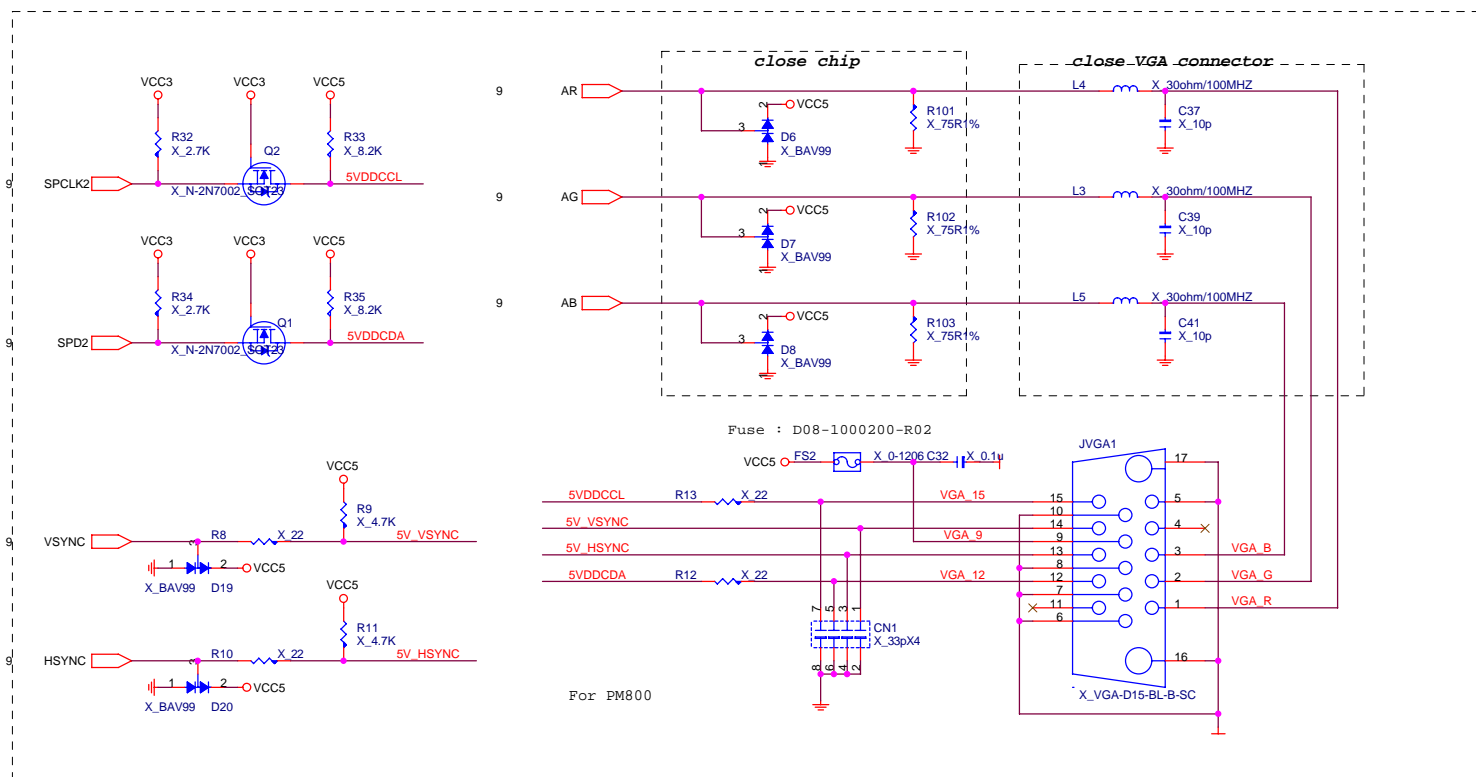
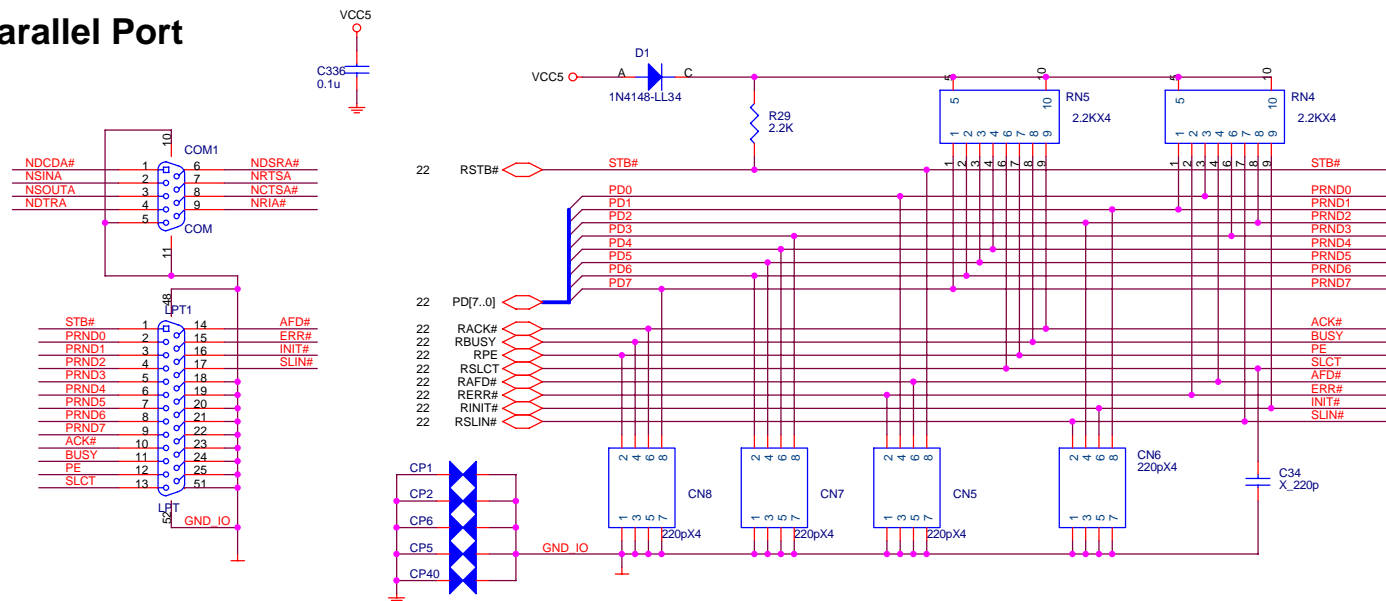
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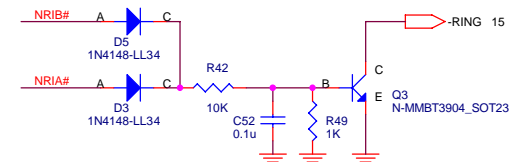
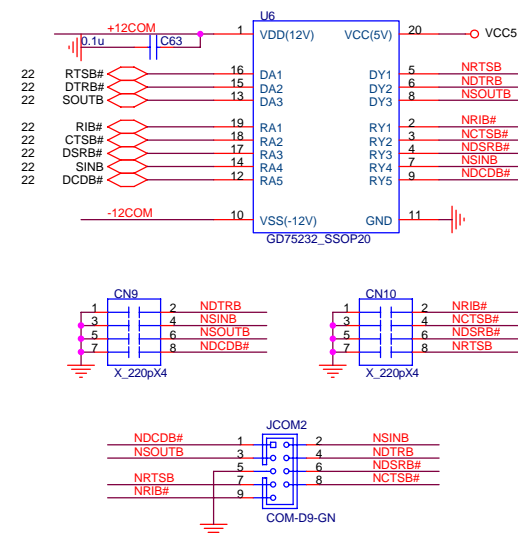
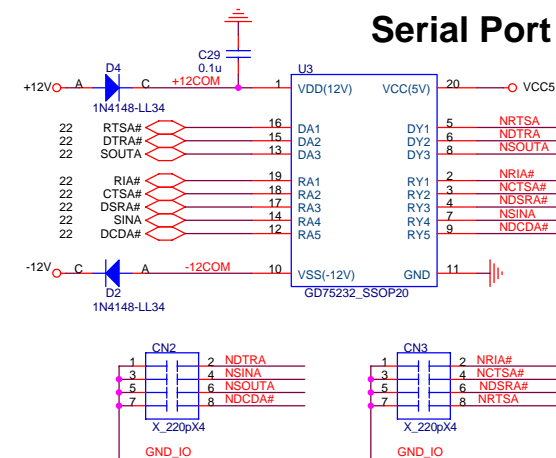
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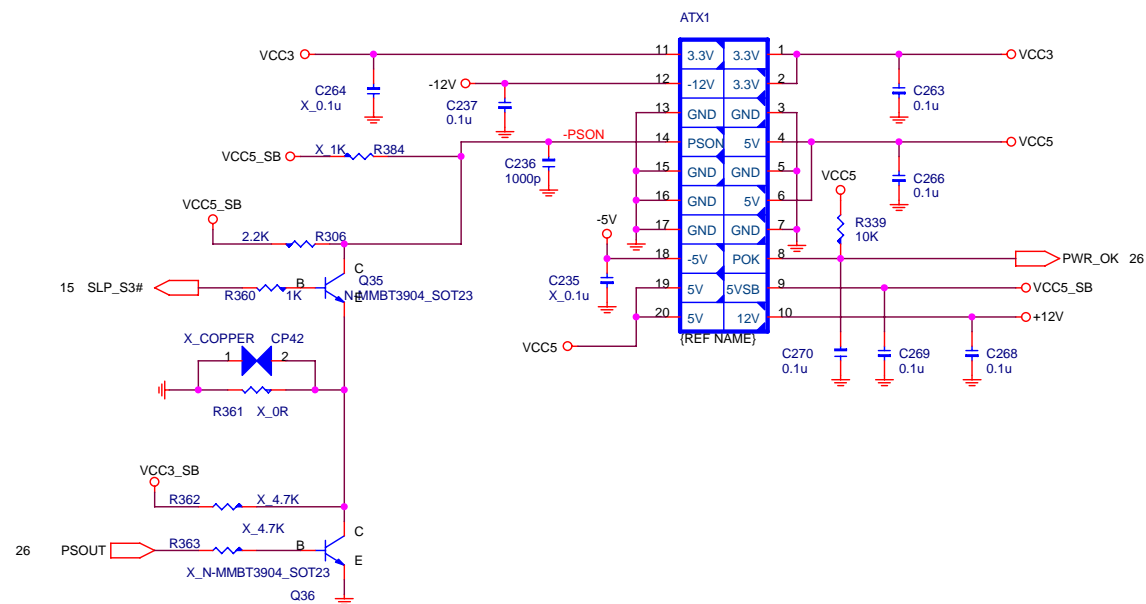
Parallel Port



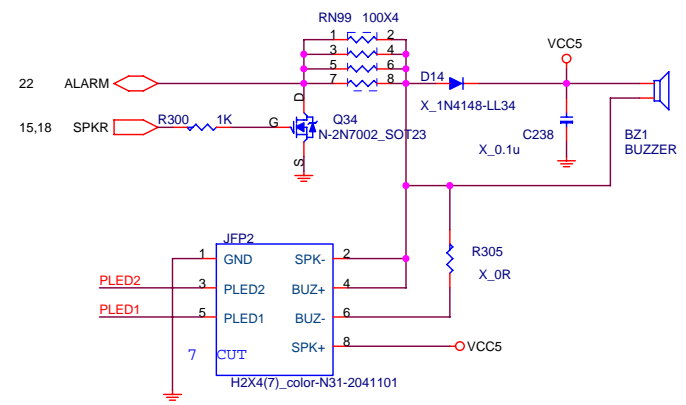
Serial Port



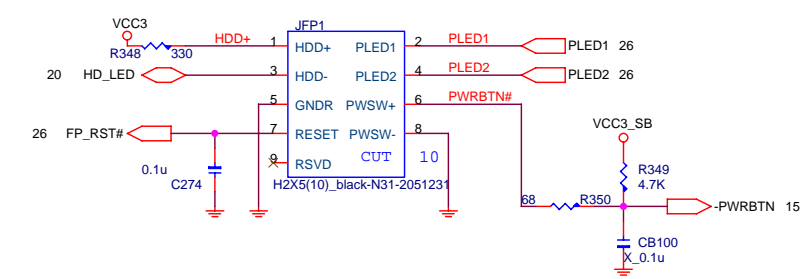
ATX Connector



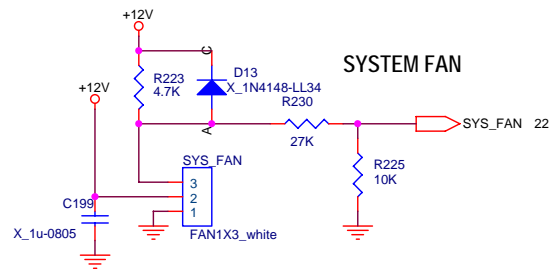
MSI Front Panel Connector



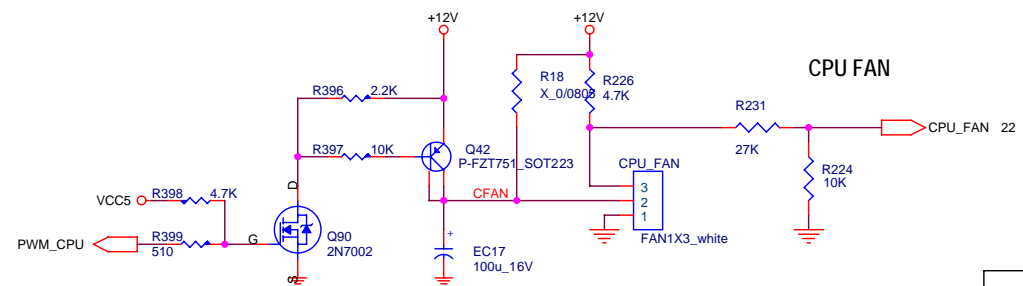
INTEL/PB Front Panel Connector



SYSTEM FAN

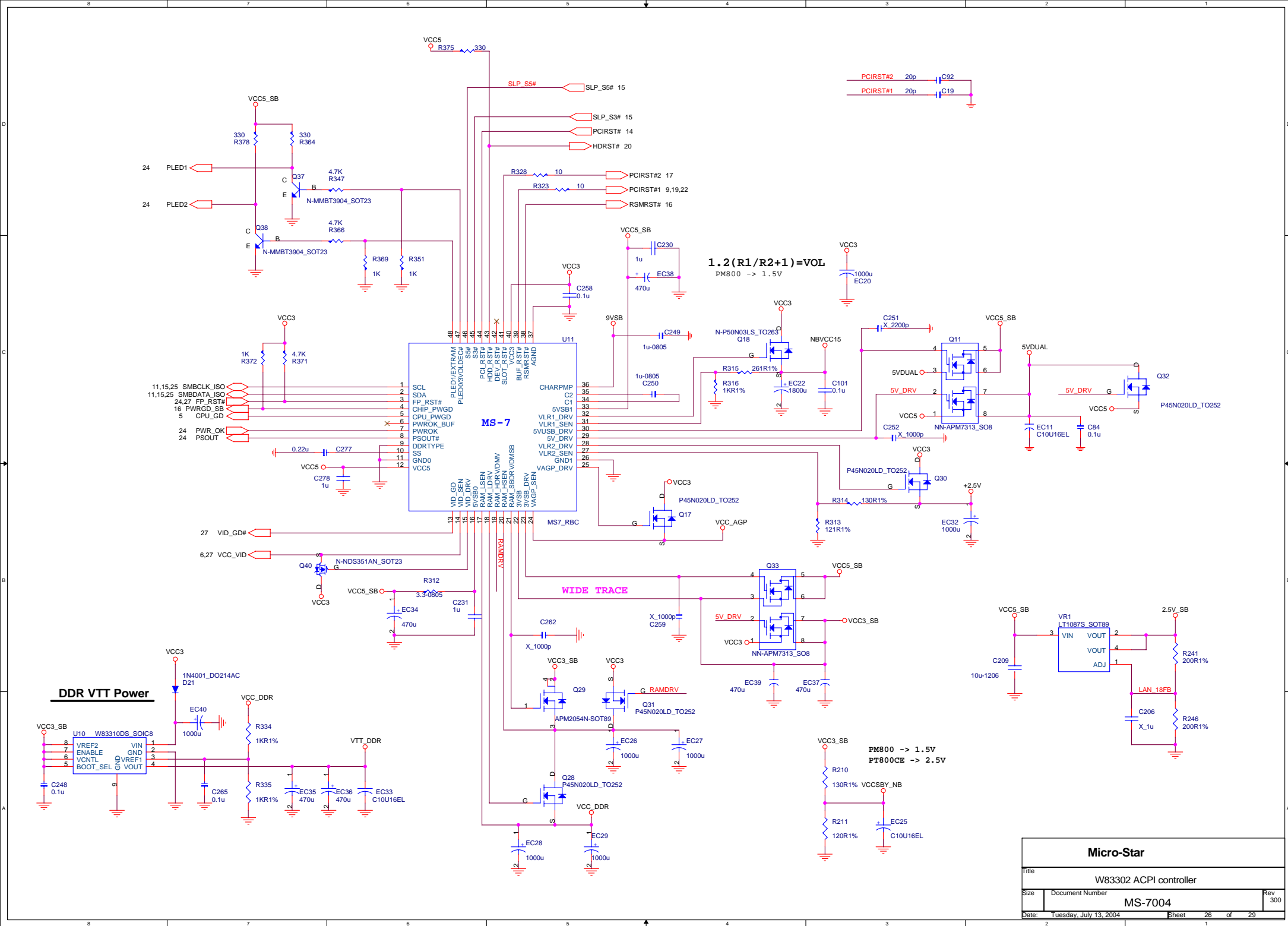


CPU FAN

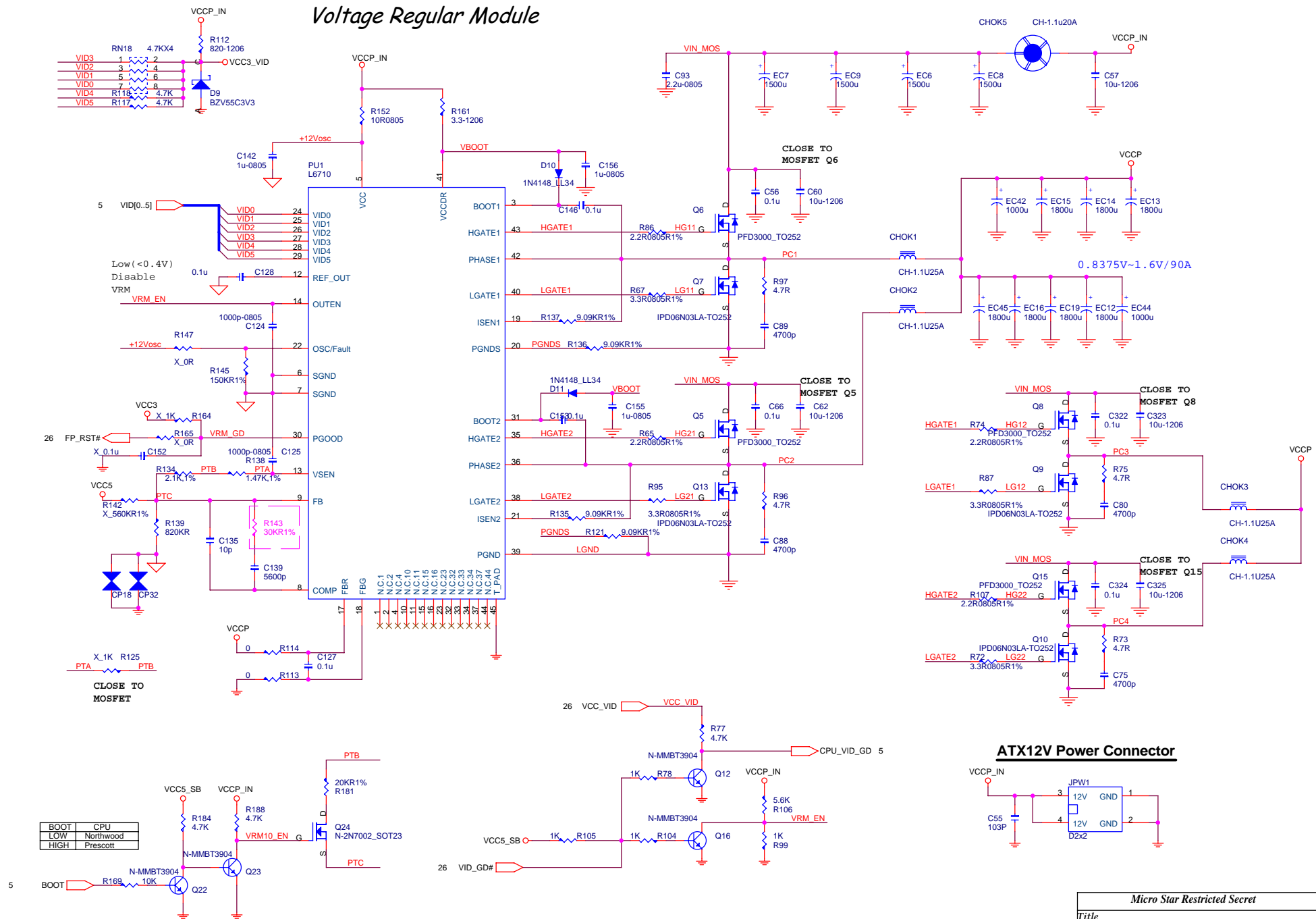


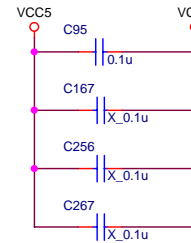
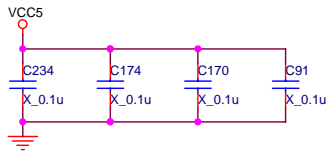
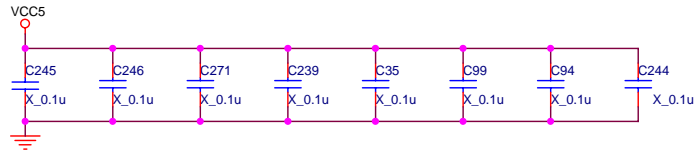
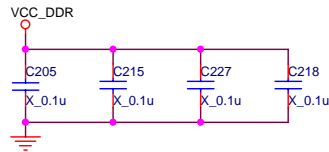
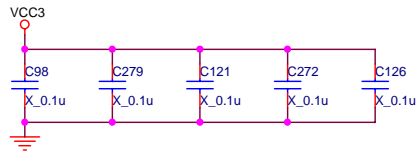
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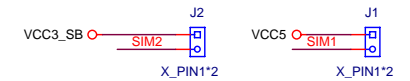


Voltage Regular Module



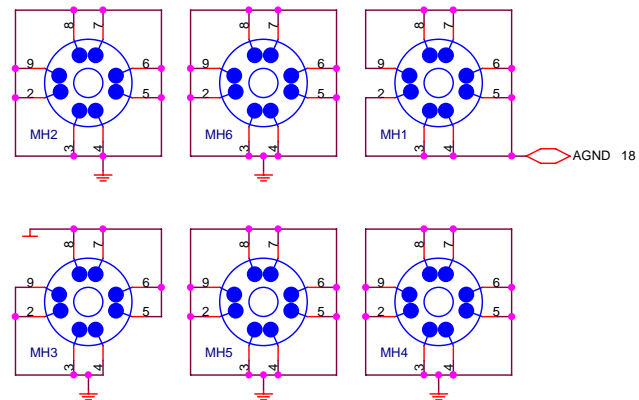
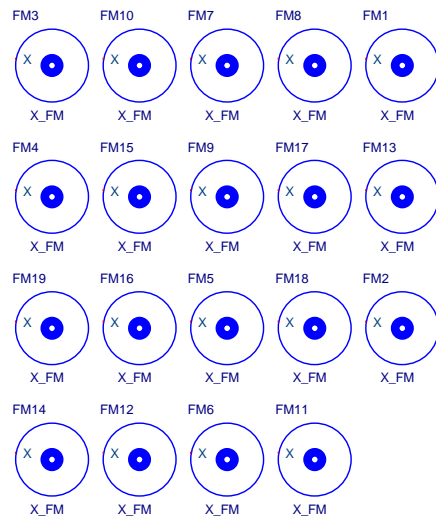


Simulation



Mounting Holes

Optics Orientation Holes



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MS-7004 V0C	
1.北橋ballout change to PM800/PT800 VER:B , Add 電源Pin .	
2.Modify PWM layout & placemant .	
3.Modify CPU & CHIPS 電源VCCP.NBVCC15內層切割.	
4.Delete 預留VT8235CE的電阻.	
5.Delete U5(Transform),改用有包進去的Lan connector .	
6.BIOS ROM 與 FANCPU1 卡機構問題 & CPUFAN 與 SYSFAN 互換	
7.Modify NB VCCDAC & VCCPLL 線路.	
8.NB 電源背焊電容改成10u/0805.	
9.Modify U8(Clock Generator)電源線路,Add ICS strapping resistors.	
10.加粗VCC5_SB & VCC3_SB切內層	

MS-7004 V100	
1.Modify net VID_GD# circuit	
2.Change some resistors & cap for VRM transient.	
3.加寬 net CPU_TMPA(CPU to I/O) & VCCP_IN(JPW1 to PU1)	
4.Modify VRM layout	
5.ADD NB pin Y6,AB5,AB6 pull down resistors & pin N3接地	
6.DDR BUS 0 ohm 直接短路	
7.C92,C19移至U11端,ADD C334 for net DCLKO	
8.Bios Rom VCC5 trace 拉至C42	
9.R389,R390,R249,R361 直接短路,cost down 0 ohm	
10.USB 0 ohm 排阻直接短路	
11.Modify VCC5 Plane for IDE BUS 跨切割	
12.VCC5 trace 拉粗至12~25 mils	
13.Modify net CPU_GD & VCC_VID & VCC_AGP_SEN & VTIN_GND 走線	

MS-7004 V10A	
1.ADD IDE 排阻	
2.Modify LAN 10/100 燈號線路	
3.Modify VRM 切割	
4.Delete JSLP1	
5.Modify +2.5V 切割區 & USB 5VDAUL 切割區	
6.change USB Rset >>> 5.9K & VGA Rset >>> 82 ohm	
7.ADD C335 20P for 北橋 PCIRST#1	
8.LVREF_SB >>> 0.3V (R276 >>> 412ohm)	

MS-7004 V300	
1.Add 判斷P4X533/PT800線路	
2.LAN change to RTL8100C(PCI)	
3.Delete CNR	
4.Update MS-7 circuit	
5.modify VRM layout	

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